



Q77H2-AM2/B75H2-AM2

Rev:1.0.

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NOTE:

Design by
473718_Maho Bay Desktop Platform and Carlow Workstation Platform PDG
474146_Intel® 7 Series/C216 Chipset Family Platform Controller Hub (PCH) EDS
1.8
MahoBay_CRB_Rev0.7

REVISION HISTORY:

Rev	Date	Notes
V.A	2011/10/12	Initial version
V.B	2011/12/09	add Power&EMI solution
V1.0	2012/1/30	add Power&EMI&SI solution
	2012/03/27	release DCN_3592 (fix DP Dongle display issue)
V1.0.	2012/04/06	release DCN_3647 (update PCB U29 footprint to fix USB3.0 LPS issue)

Table 1-2. Intel® 7 Series Chipset Family SKUs

Feature Set	SKU Name					
	Intel® Q77 Express Chipset	Intel® Q75 Express Chipset	Intel® B75 Express Chipset	Intel® Z77 Express Chipset	Intel® Z75 Express Chipset	Intel® H77 Express Chipset
PCI Express* 2.0 Ports	8	8	8	8	8	8
PCI Interface	Yes	Yes	Yes	No ²	No ²	No ²
Total number of USB ports	14	14	12 ⁴	14	14	14
• USB 3.0 Capable Ports (SuperSpeed and all USB 2.0 speeds)	4	4	4	4	4	4
• USB 2.0 Only Ports	10	10	8	10	10	10
Total number of SATA ports	6	6	6	6	6	6
• SATA Ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s)	2 ⁵	1 ⁶	1 ⁶	2 ⁵	2 ⁵	2 ⁵
• SATA Ports (3 Gb/s and 1.5 Gb/s only)	4	5	5	4	4	4
HDMI/DVI/VGA/DisplayPort*/eDP*	Yes	Yes	Yes	Yes	Yes	Yes
Integrated Graphics Support	Yes	Yes	Yes	Yes	Yes	Yes
Intel® Rapid Storage Technology	AHCI	Yes	Yes	Yes	Yes	Yes
	RAID 0/1/5/10 Support	Yes	Yes ⁷	No	Yes	Yes
Intel® Anti-Theft Technology	Intel® Smart Response Technology	Yes	No	Yes	No	Yes
		Yes	Yes	Yes	Yes	Yes
Intel® Active Management Technology 8.0	Yes	No	No	No	No	No
Intel® Small Business Advantage	Yes ⁸	No	Yes	No	No	No
Intel® Rapid Start Technology ⁹	Yes	Yes	Yes	Yes	Yes	Yes
ACPI S1 State Support	Yes	Yes	Yes	Yes	Yes	Yes

NOTES:

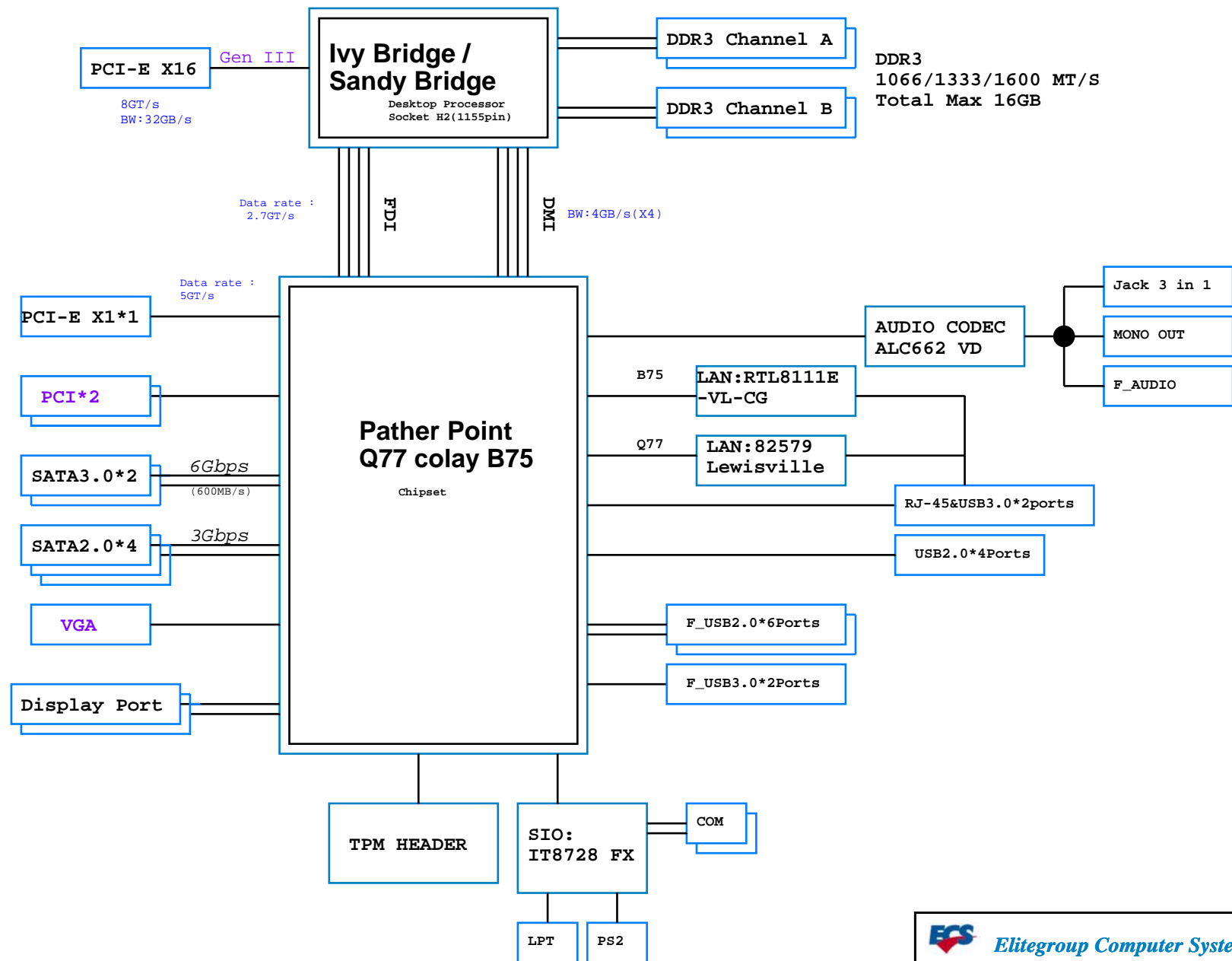
1. Contact your local Intel Field Sales Representative for currently available PCH SKUs.
2. Table above shows feature differences between the PCH SKUs. If a feature is not listed in the table it is considered a Base feature that is included in all SKUs.
3. PCI Legacy Mode may optionally be used allowing external PCI bus support through a PCIe-to-PCI bridge. See Section 5.1.9 for more details.
4. USB ports 6 and 7 are disabled.
5. SATA 6 Gb/s support on port 0 and port 1. SATA ports 0 and 1 also support 3 Gb/s and 1.5 Gb/s.
6. SATA 6 Gb/s support on port 0 only. SATA port 0 also supports 3 Gb/s and 1.5 Gb/s.
7. Supports RAID 1 only.
8. Intel® Small Business Advantage with the Intel® Q77 Express Chipset requires an Intel® Core™ iPro™ processor.
9. Intel® Rapid Start Technology requires an appropriate processor be installed in the platform. See processor collaterals for further details.



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Cover Page

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PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO1	VCC3	OBR	GPI
GPIO6	VCC4	Over_temp	GPI
GPIO12	3VSB	LAN_DISABLE_L	Native
GPIO13	3VSB	LPC_PME_L	GPI
GPIO23	VCC3	HDPANEL_DETECT	Native
GPIO24	3VSB	USB Power Control	GPO
GPIO27	SB_3VSB	DEEP LANWAKEB	GPI
GPIO45	3VSB	SPI_WPSW	Native
GPIO57	3VSB	SPI_WP0_L	GPI
GPIO59	3VSB	LAN_LED_D	Native
GPIO61	3VSB	LPCPD_L	Native
GPIO72	3VSB	USB Power Control	GPO

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO14		Over_temp	
GPIO34		MB_ID1	
GPIO16		SIO_BEEP	
GPIO22		SIO_LED1	
GPIO23		SIO_LED0	
GPIO35		MB_ID2	
GPIO36		GPO36 FOR ACER reserve	
GPIO40		5VDAUL_MEM Control	
GPIO64		GPO64 FOR ACER reserve	
GPIO47		TP_VGA	

Straping Table

FCH Straping (Page.14)

TLS Confidentiality:

TLS_EN (internal PD)	
H	Enable TLS
L	Disable TLS

No Reboot:

PCH_SPKR (internal PD)	
H	Enable No Reboot
L	Disable

On-Die PLL VR:

ON_DIE_PLL_EN (internal PU)	
H	Enable
L	Disable

On-Die PLL VR Source:

HDA_SYNC_R (internal PD)	
H	1.5V
L	1.8V

Integrated 1.05V SUS VRM:

INTVRMEN	
H	Enable
L	Disable

SIO IT8728F D/EX/FX Straping (Page.26)

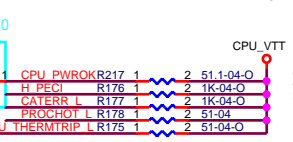
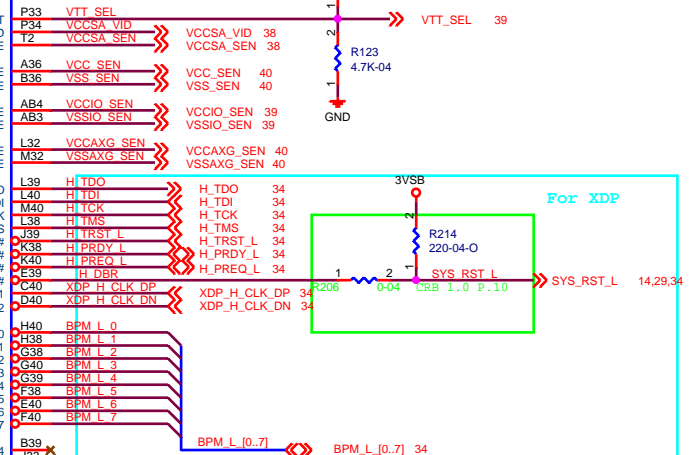
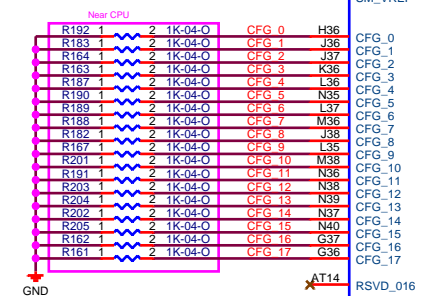
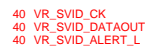
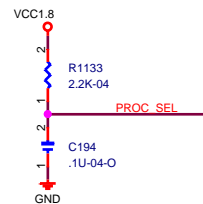
Power-On Strapping

	Symbol	Value	Description
JP1	DSW_EUP_SEL	1	EUP
Pin-48		0	DSW
JP2	WDT_EN	1	Disable WDT to reset PWROK
Pin-122		0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1	EC Index 63h/6Bh/73h is 80h
Pin-124		0	EC Index 63h/6Bh/73h is 00h
JP4	K8PWR_EN	1	Disable K8 Power Sequence
Pin-126		0	Enable K8 Power Sequence
JP5	UOVMODE_SEL	1	Notice Mode (Default)
Pin-29	OV/UV	0	Force Mode

* Port 1 or Port 9 is USB 2.0 Debug Port

Panther point INT# Table

Function	INT Port	PCI-EX1 Port	Chip
Lan Ethernet Controller	INTC# (Default)	Port3	Intel 82579LM / Realtek RTL8111E
SATA 1&2 Controller (IDE Mode)	INTB# (Default)	NA	PCH intergrated
PCIEX Slot	INTD# (Default)	Port4	External PCIEX Card



MCPU DIMM

Diagram illustrating the connection of the CPU DIMM to the system. The DIMM is connected to the CPU via a 10 mils trace. The connection is labeled **DIMM VREF_CPU**. The DIMM is connected to GND through a network of resistors (R281, R278) and capacitors (SC84).

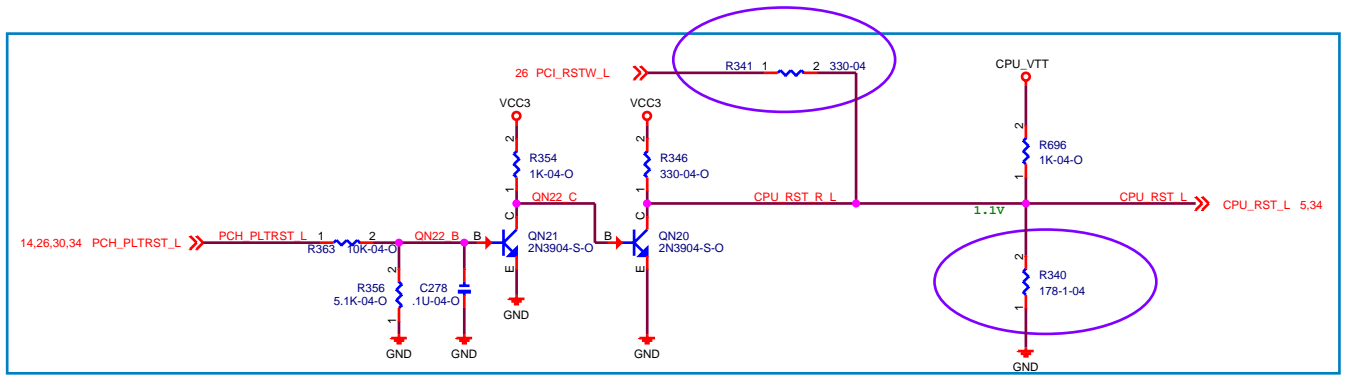
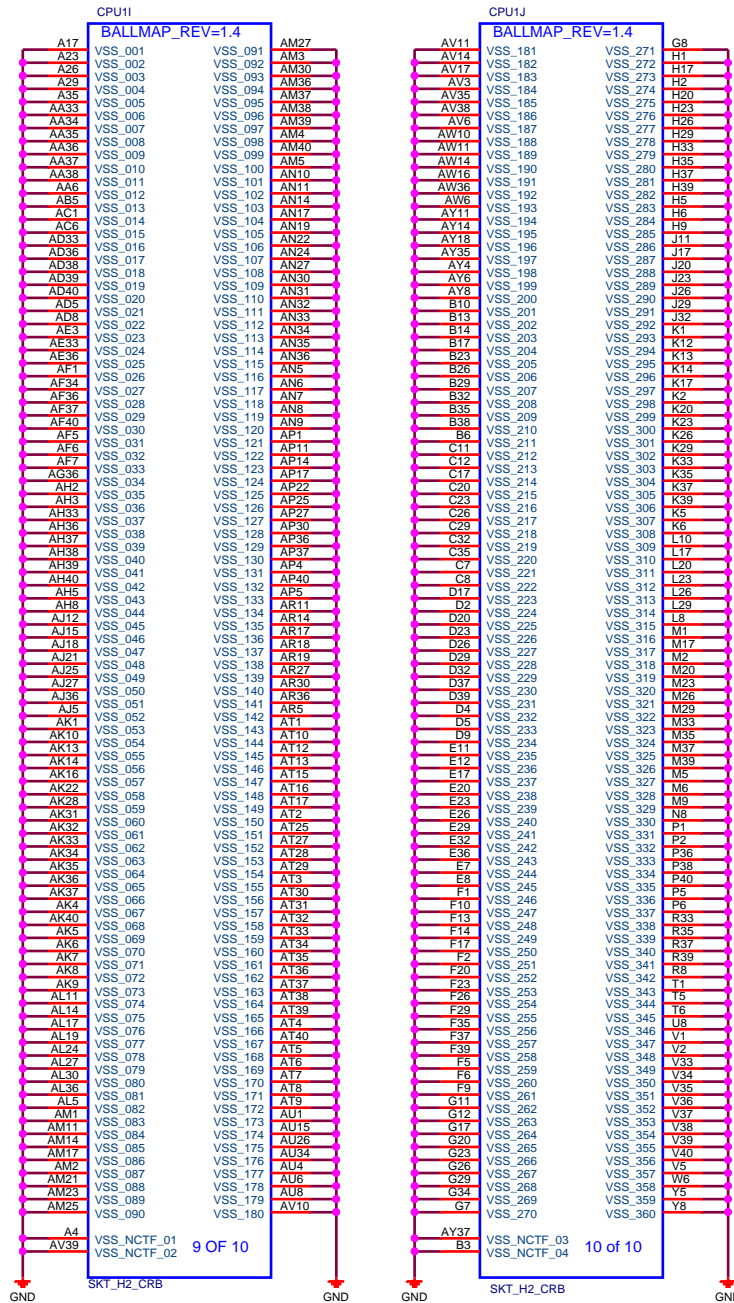
Layout Note:
All Parts Close yo CPU

DIMM_VREF_CPU Control Mode:

Control Mode Part	Divider	PCH + Controller
Mcpu	X	V
Ncpu	X	V
Pcpu	V	X

Default

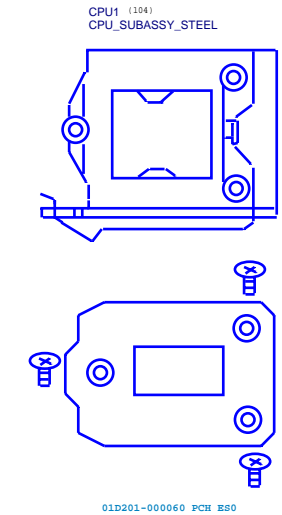
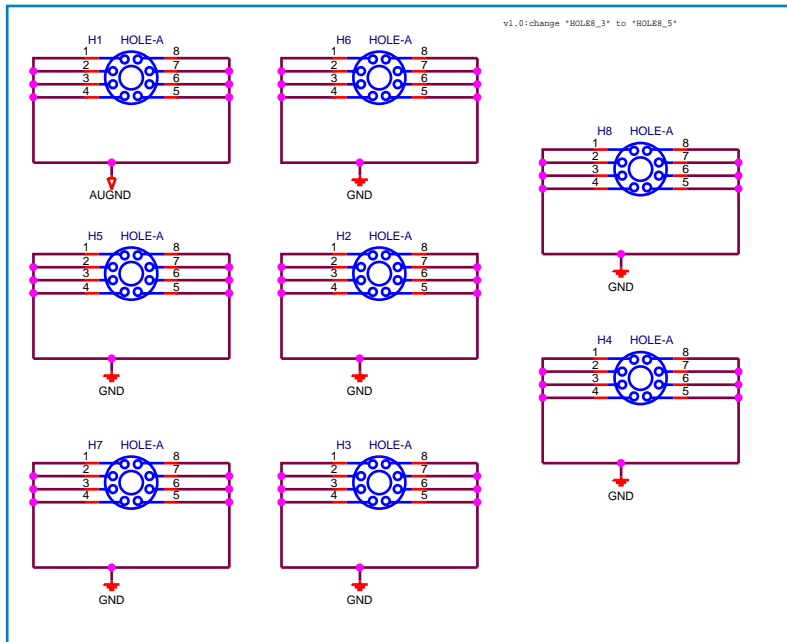
CFG[5:6]:
11=DEFAULT X16,
01=2X8,
10=RESERVED,
00=X8,X4,X4

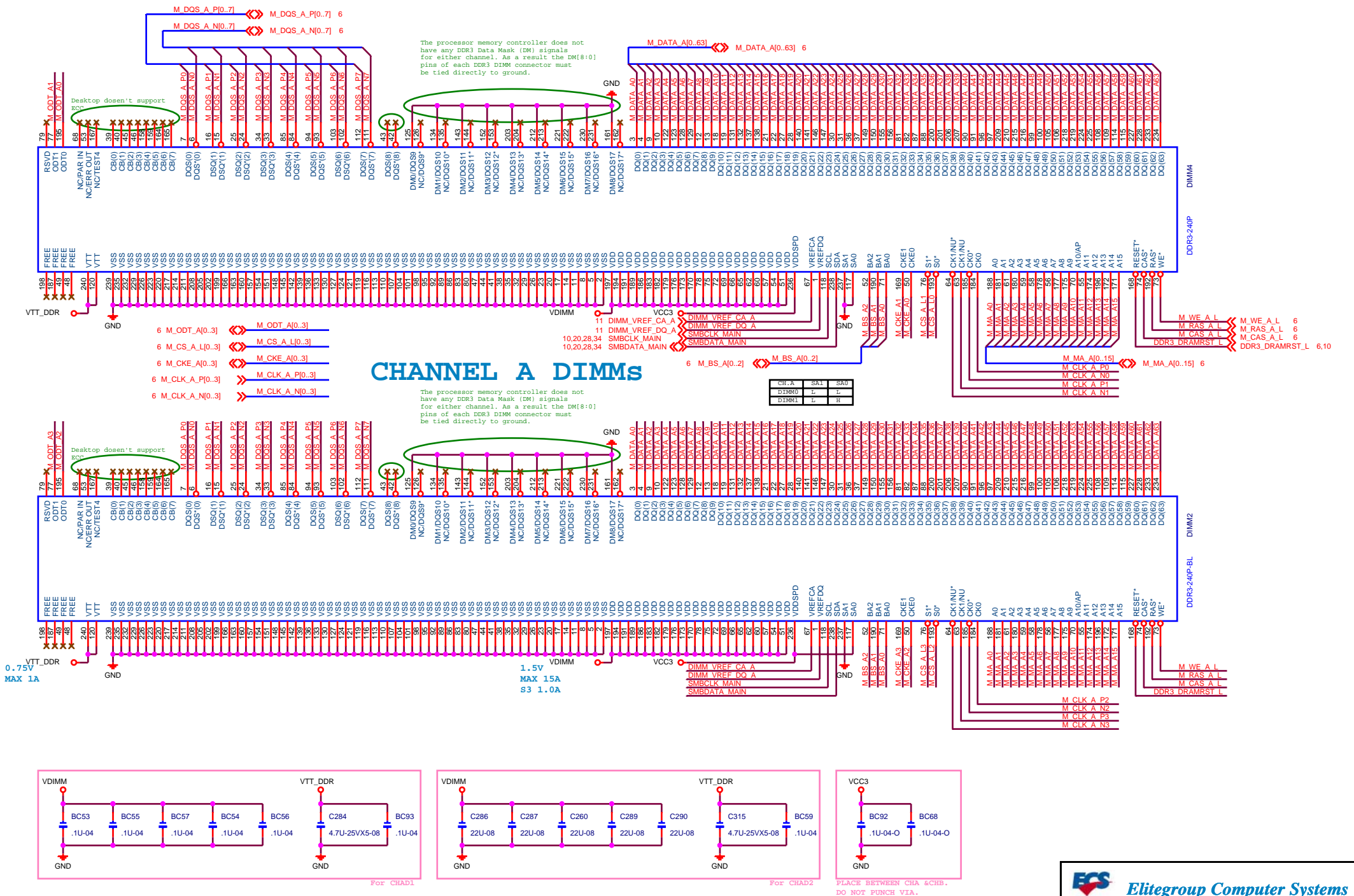


V1.0.
 15-RE11-011090
 PCB M/B.Q77H2-AM2/B75H2-AM2.V1.0
 (...)...244*244*1.6mm.4L...LEAD-FREE
 (ROHS).GREEN.OSP.....GEI

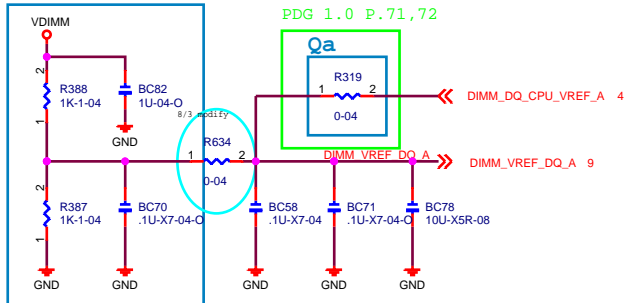
11-018-115123 SOCKET.CPU..LGA
 1155P SMD..G/F...BLACK.ACA-ZIF-096-R02..
 ...LEAD-FREE(ROHS/HP).LOTES

20-800-006211 SUBASSY.STEEL....LGA 1155/11
 56P.W/BACK PLATE,CAP.ACA-ZIF-082-E32.....
 LEAD-FREE(ROHS/HP).LOTES



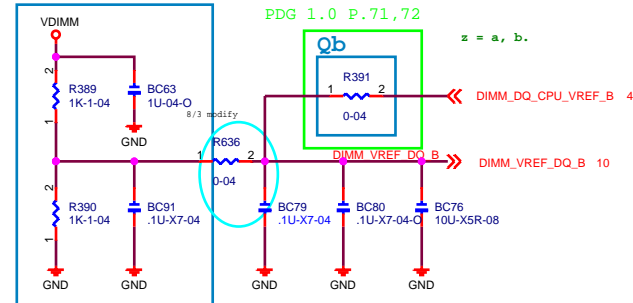


Pa



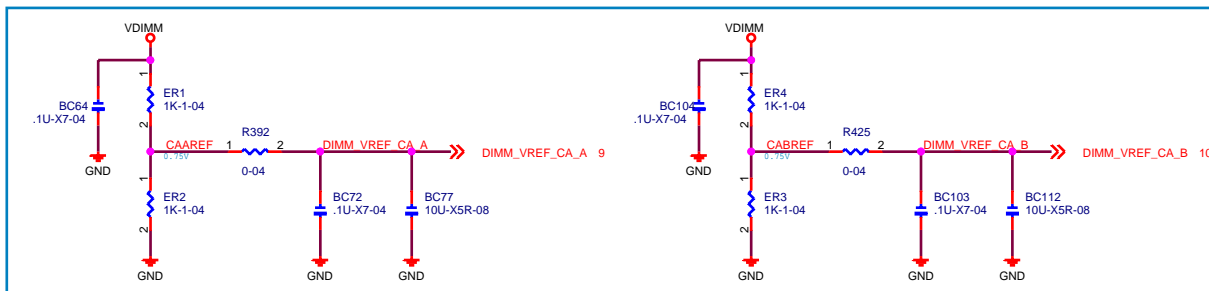
2011.08.25 Remove Divider Control Circuit

Pb



Layout Note:
All parts close to DDR3 Slots.

DIMM_VREF_DQ Control Circuit

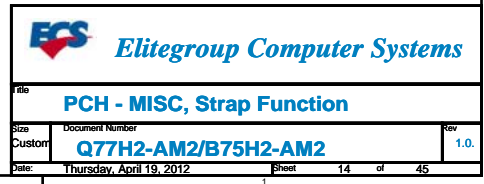


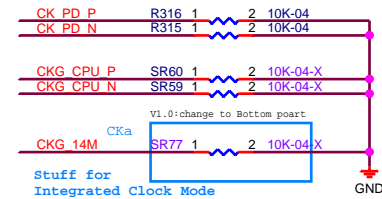
DIMM_VREF_CA Circuit



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PCB Layout for PCH1H

Top Section:

- Left:**
 - 28 TCM33M: TCM33M R, AT11
 - 26 SIO_33M: SIO_33M R, AN14
 - 12 PCI_33M_FB: PCI_33M_FB R, AT12
 - 21 PCIB33M: PCIB33M R, AT17
 - 21 PCIA33M: PCIA33M R, AT14
- Right:**
 - CLKOUT_PCI0
 - CLKOUT_PCI1
 - CLKOUT_PCI2
 - CLKOUT_PCI3
 - CLKOUT_PCIL00BACK
 - CLKOUTFLEX0_GPIO64
 - CLKOUTFLEX1_GPIO65
 - CLKOUTFLEX2_GPIO66
 - CLKOUTFLEX3_GPIO67

Bottom Section:

- Left:**
 - 26 SIO_48M: SIO_48M R, AN8
 - XCLK_RCOMP: CKG 14M, AL2
- Right:**
 - CLKIN_GND1_N
 - CLKIN_GND1_P
 - CLKIN_GND0_N
 - CLKIN_GND0_P
 - CLKOUT_ITPXPDP_N
 - CLKOUT_ITPXPDP_P
 - CLKOUT_PCIE7N
 - CLKOUT_PCIE7P
 - CLKOUT_DMI_N
 - CLKOUT_DMI_P
 - CLKOUT_DP_N
 - CLKOUT_DP_P
 - CLKOUT_PCIE0N
 - CLKOUT_PCIE0P
 - CLKOUT_PCIE1N
 - CLKOUT_PCIE1P
 - CLKOUT_PCIE2N
 - CLKOUT_PCIE2P
 - CLKOUT_PCIE3N
 - CLKOUT_PCIE3P
 - CLKOUT_PCIE4N
 - CLKOUT_PCIE4P
 - CLKOUT_PCIE5N
 - CLKOUT_PCIE5P
 - CLKOUT_PCIE6N
 - CLKOUT_PCIE6P
 - CLKOUT_PEG_A_N
 - CLKOUT_PEG_A_P
 - CLKOUT_PEG_B_N
 - CLKOUT_PEG_B_P

Crystal Circuit Diagram:

XTAL 25M PCH OUT AJ5
XTAL 25M PCH IN AJ3
XTAL25_OUT
XTAL25_IN

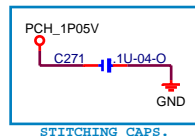
Only can use 0603 type.

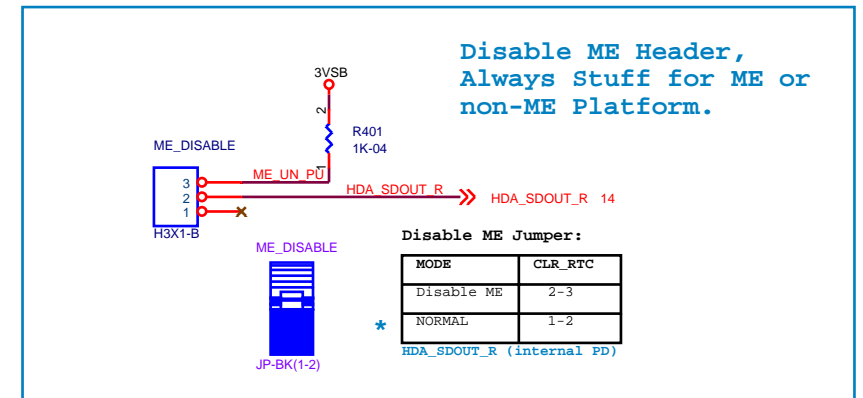
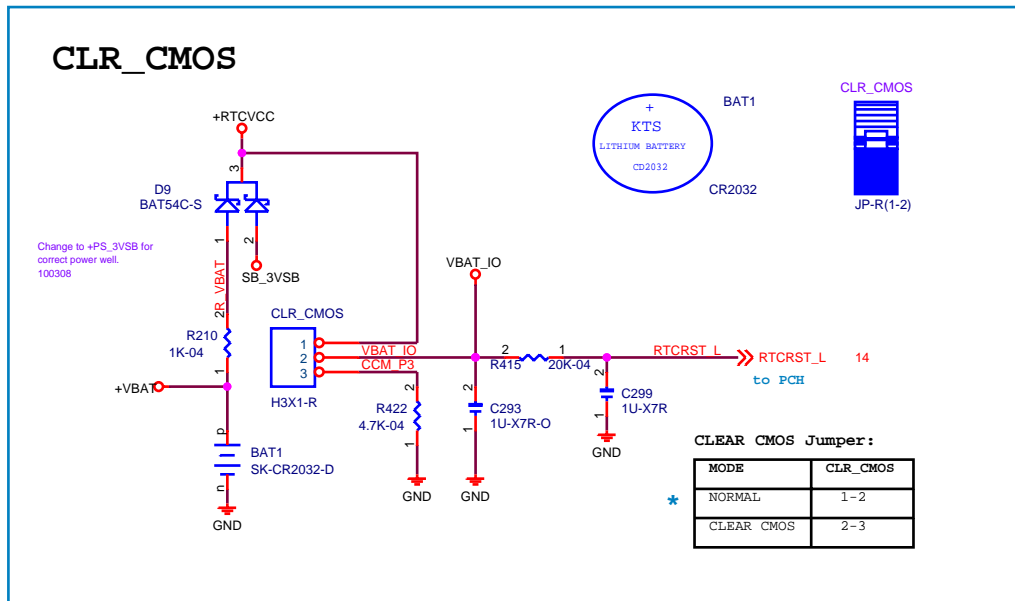
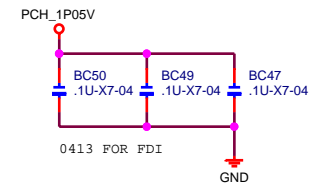
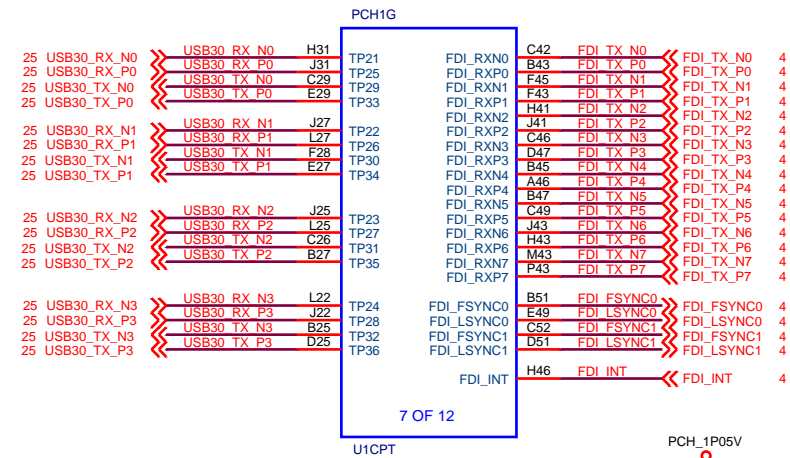
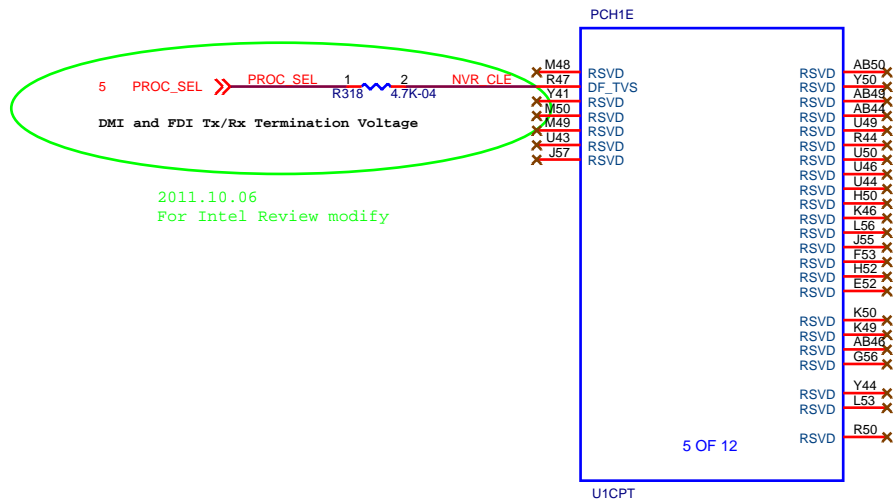
XTAL, 25MHZ, 30ppm, 20pF

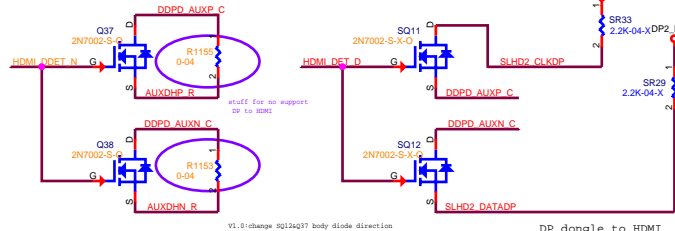
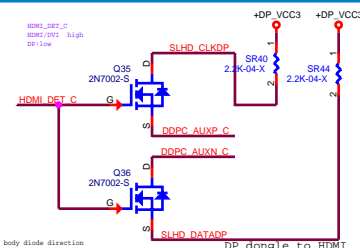
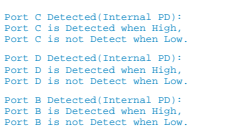
Components: R245 (1M), X2 (X-25M), C206 (27P-04), C199 (27P-04), GND.

Other Labels:

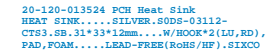
- 8 of 12
- U1CPT
- VCC3
- PCH_1P05V

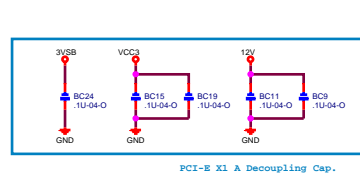
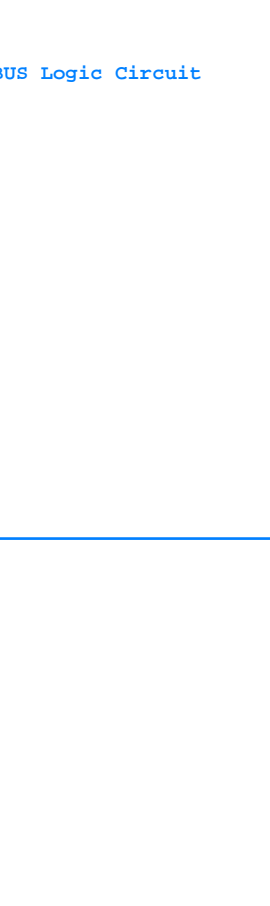




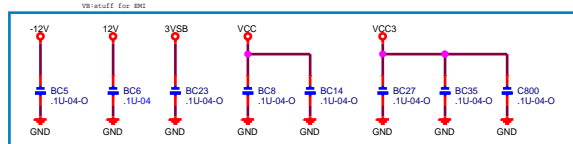
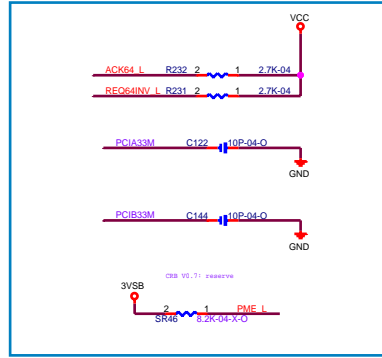
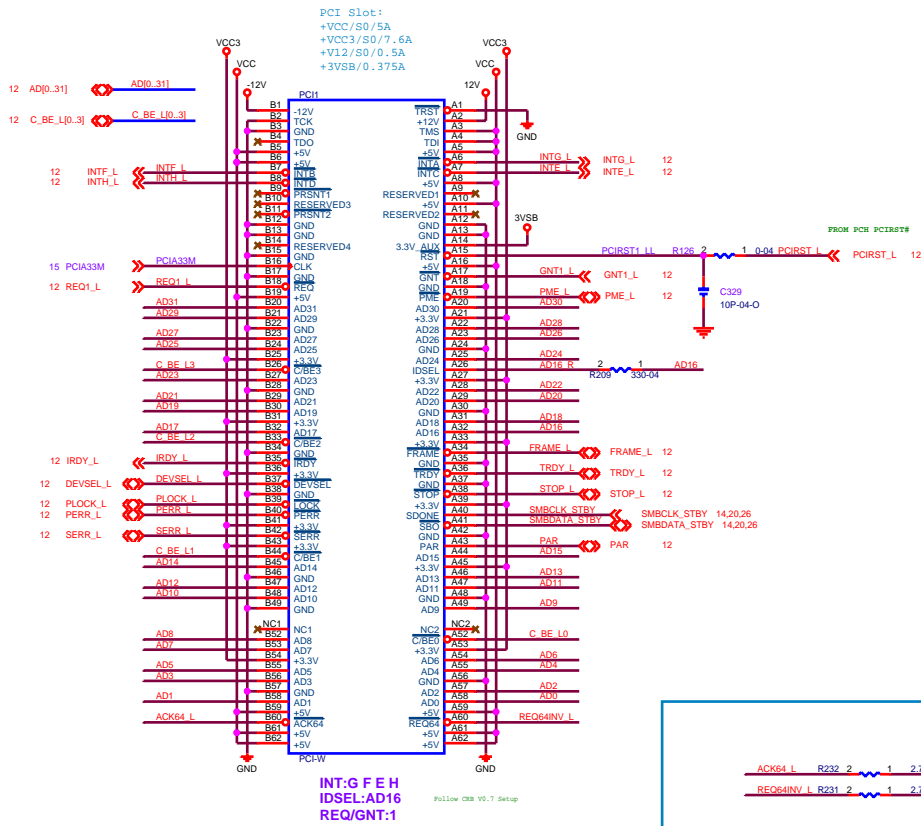




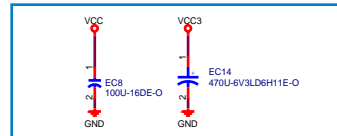




PCI V2.3

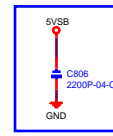
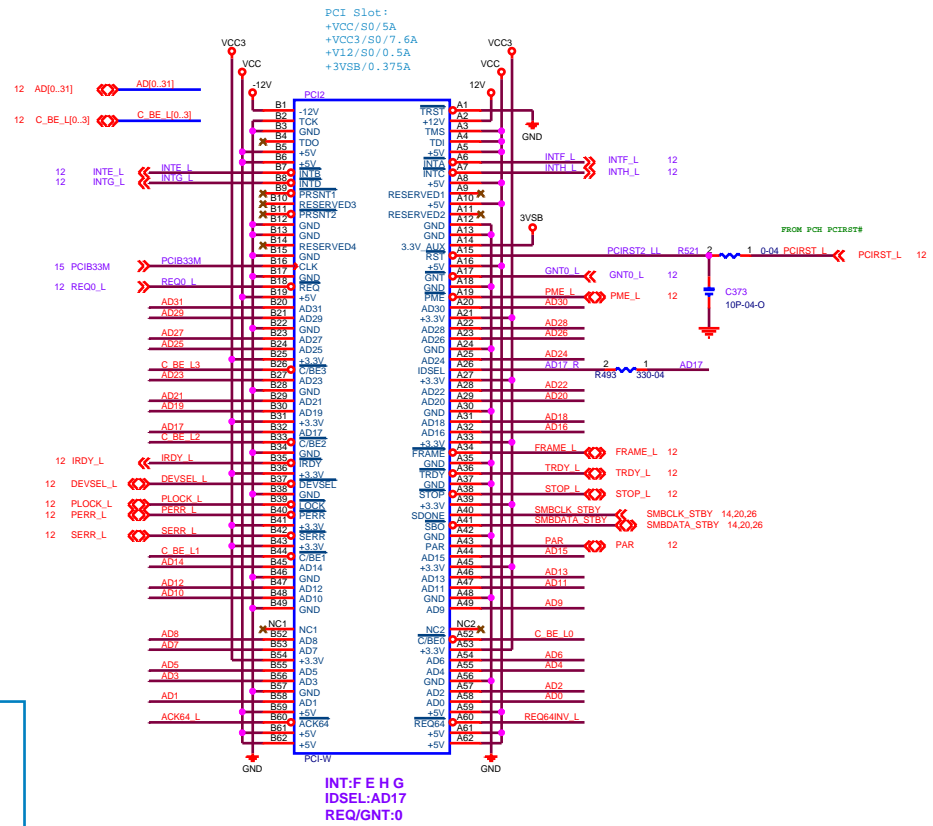


PCI1 Decoupling Cap.

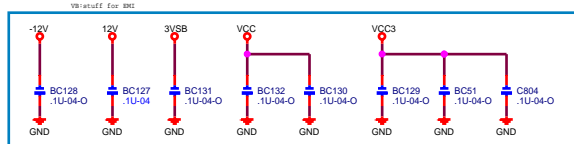


PCI1&2 Decoupling Cap.

PCI V2.3



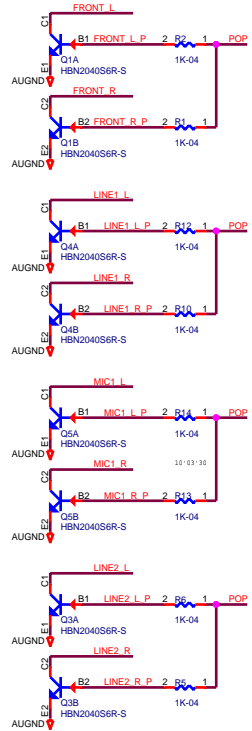
VB+add reserve for BMC
AM stuff it



PCI2 Decoupling Cap.

Depop schematic

The schematic shows a 3VSB input connected to a network of resistors (R75, R76, R74, R65, R64) and MOSFETs (Q9, Q10, Q8). The circuit includes nodes labeled POP_1, POP_2, POP_3, and ANTI_POP_R. A 220K-04 resistor is connected to the 3VSB output. The schematic is labeled "Depop schematic".



PORT-E&P

23 LINE2_ID

23 MC2_ID

23 FRONT_L

23 FRONT_R

10/12 modify control

23 FRONT_L2

23 FRONT_R2

23 FRONT_L1

23 FRONT_R1

23 SENSE-B

23 R29 1 2 39.2K-104

23 R22 1 75-04

23 R23 1 75-04

23 EC13 1 100U16DE-05

23 EC19 1 100U16DE-05

23 20K-104

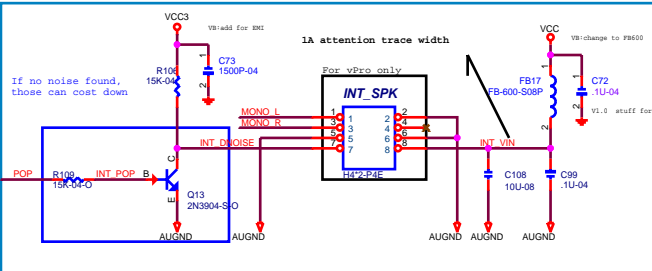
MONO L C42 1 2 1U MONO L C 39
 AUGND R61 2 20K-1.04 JDRF 40
 MONO R C50 1 2 1U MONO R C 41
 AUGND

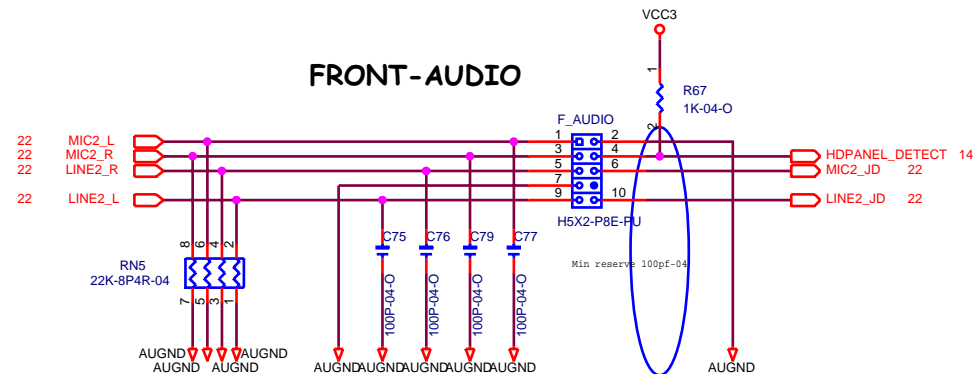
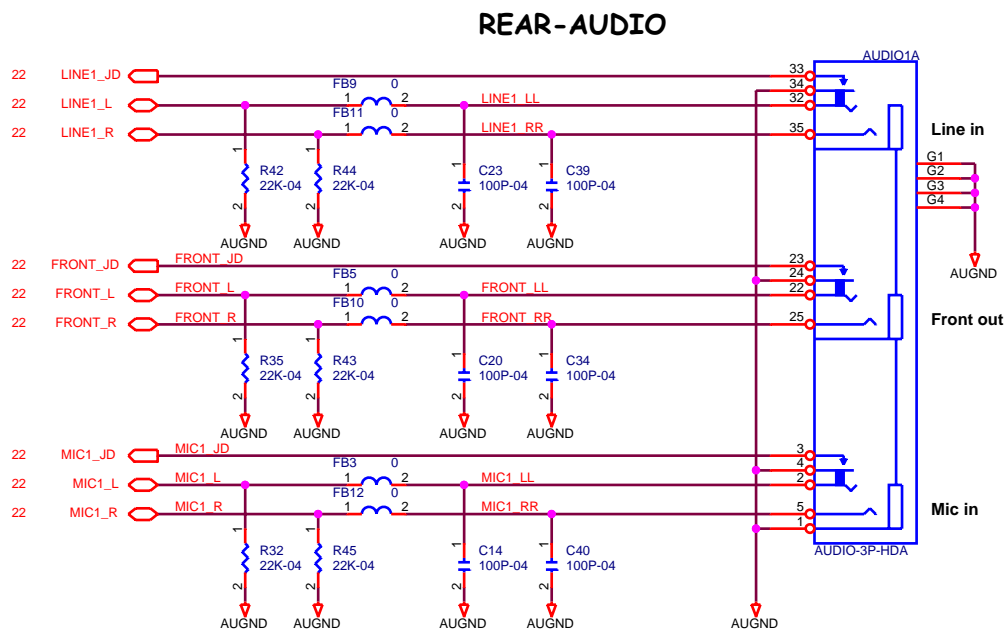
C36 1U-04 SC23 10U-08K-0
 AUGND AUGND

36 37 38 39 40 41
 FRONT-R FRONT-L
 VREF0
 AVDD02
 SURR-L
 JDRF
 SURR-R

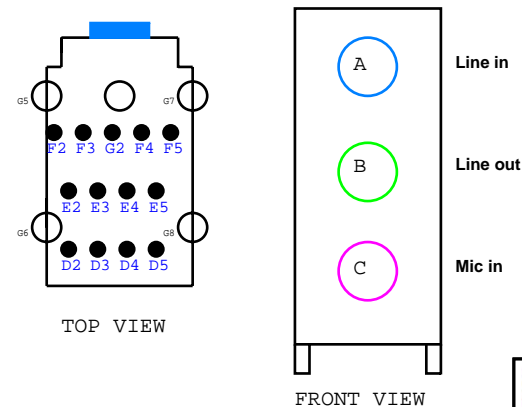
PCB layout showing the connection of the anti-pop resistor R494 to the VDD pin of the IC. The resistor is connected to the VDD pin and the ground plane. The layout includes labels for various components and pins, such as R494, VDD, GND, and the IC pins.

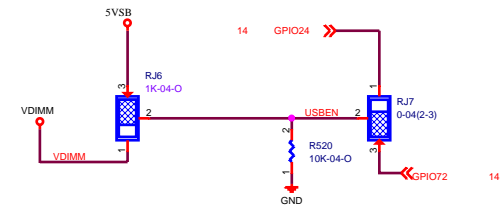
	ALC662 VC	ALC662 VD
Ca	V	X
Cb	X	V
Cc	X	V
Cd	V	X



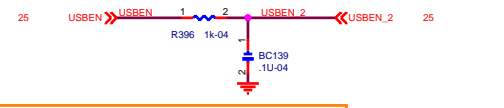


VB:remove SPDIF Circuit

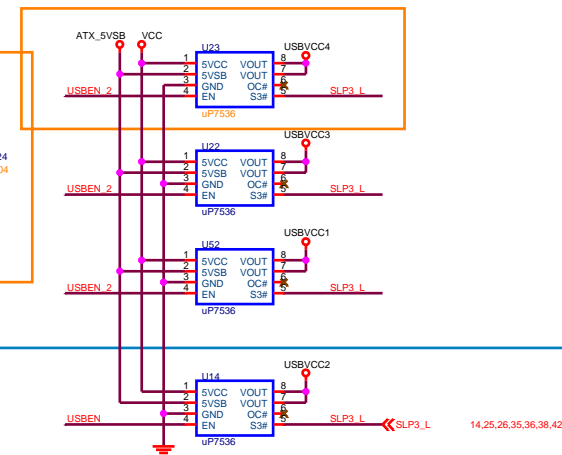




	uP7536 Enable Use	RJ6	RJ7	S4/S5 USB_5V_DUAL	Customer
	VDIMM	1K (1-2)	N A	0 Volt	Acer S4 w/o SS w/ USB_5V_DUAL
	5VSB	1K (2-3)	N A	5 Volt	
★	GPIO40_S4S5	N A	0 ohm	S4 : 0 Volt S5 : 5 Volt	

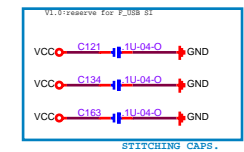


```
B75: unstuff
Q77: stuff
```

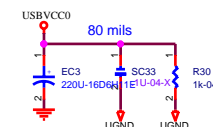


FRONT PANEL USB HEADER

REAR PANEL USB HEADER



USB2.0*4 Connector



USB3.0 Header

USB3 ESD COMPONENTS

FRONT PANEL USB3.0 HEADER

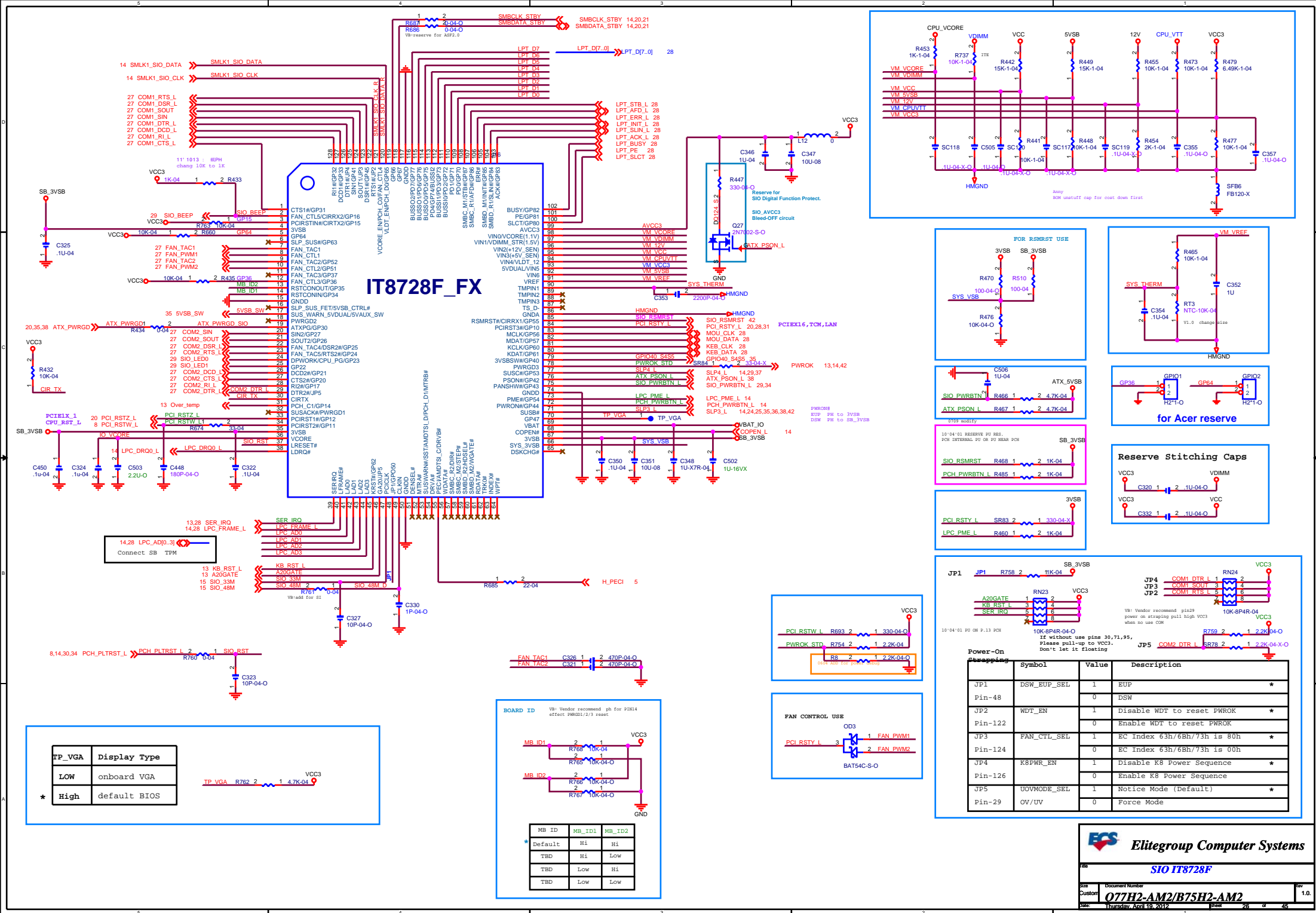
REAR PANEL USB3.0 CONNECTOR

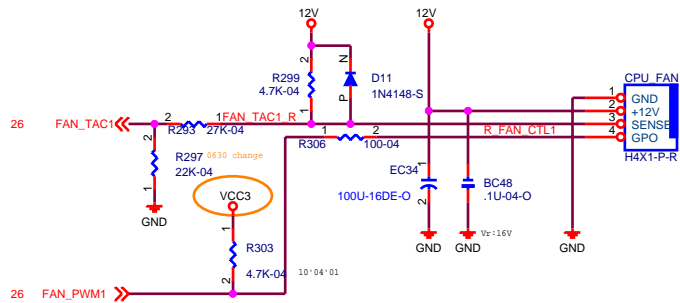
USB3.0 connector

```

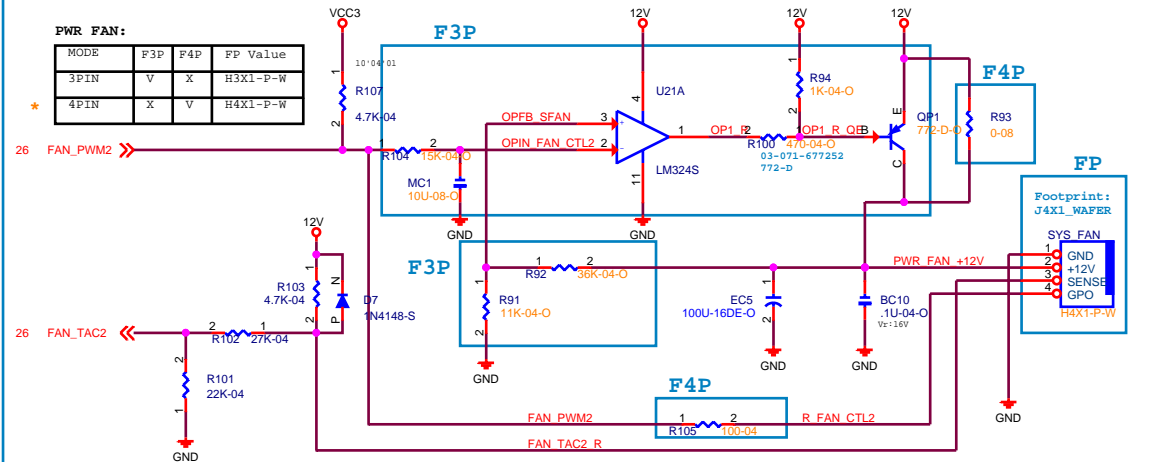
10-084-032241
CONN.USB(3.0)DUAL PORT+LAN..32P 90D....30u..
W/LED(LG-RG/O).1000 TRANS...05-000199R13-1...LEAD-FREE.UDE
盒 10-084-032901
CONN.USB(3.0) DUAL PORT+LAN..32P 90D....30u..W/LED(LG-RG/O).
1000 TRANS...PD1BE01115A5...LEAD-FREE(RoHS).ICOTHING

```



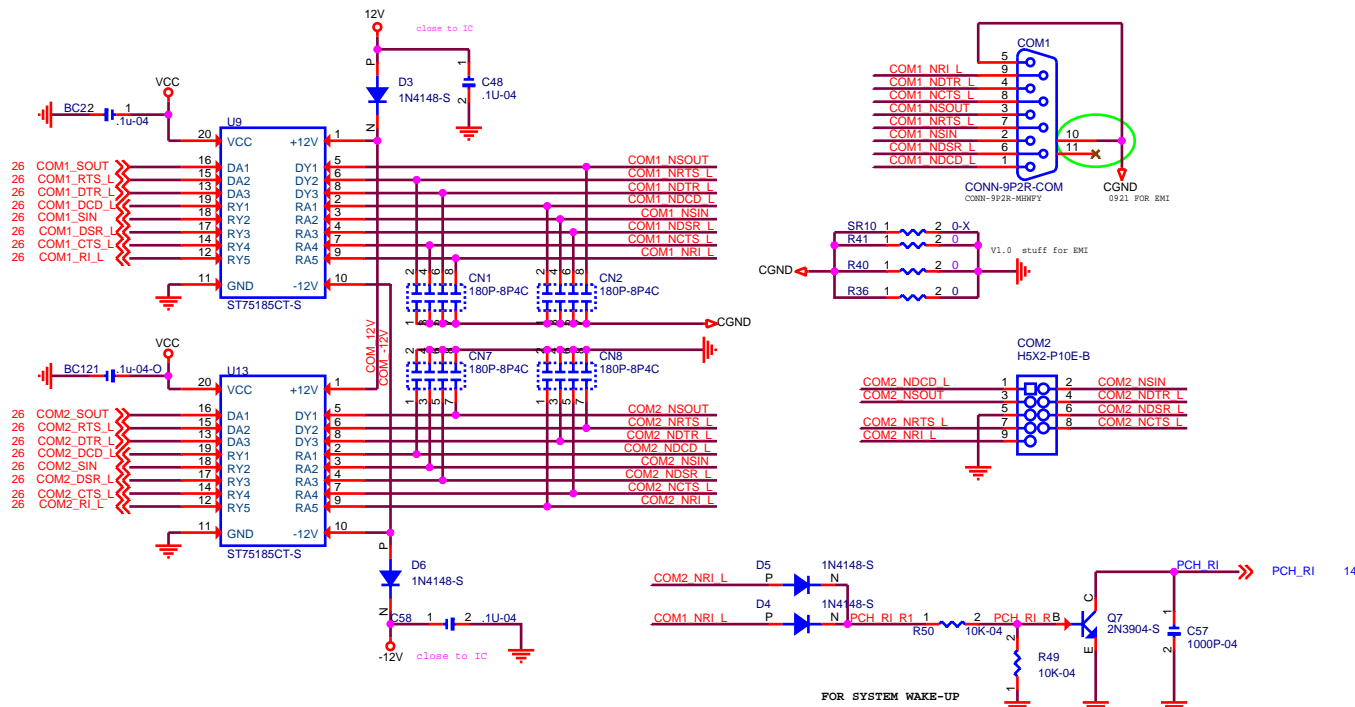


CPU FAN 4-PIN Circuit



SYS FAN 3-PIN(Co-Lay 4PIN) Circuit

COM PORT I/O



26 LPT_D[7..0] >> LPT_D[7..0]

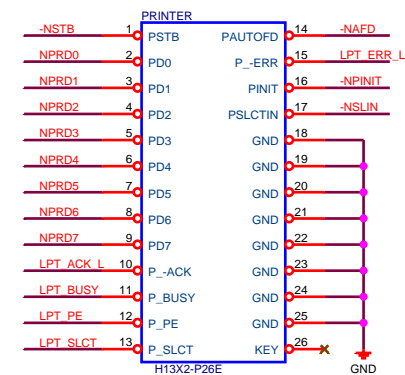
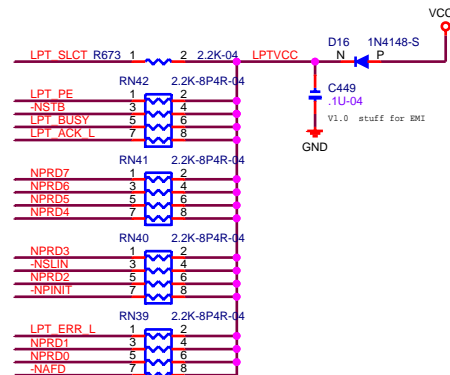
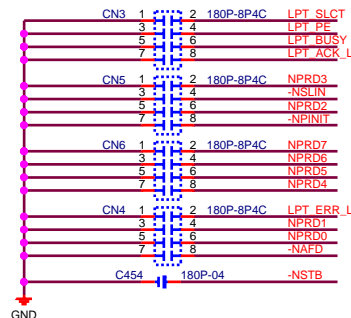
26 LPT_STB_L >> LPT_STB_L
26 LPT_ACK_L >> LPT_ACK_L
26 LPT_BUSY >> LPT_BUSY
26 LPT_PE >> LPT_PE
26 LPT_SLCT >> LPT_SLCT

26 LPT_AFD_L >> LPT_AFD_L
26 LPT_ERR_L >> LPT_ERR_L
26 LPT_INIT_L >> LPT_INIT_L
26 LPT_SLIN_L >> LPT_SLIN_L

LPT D1 RN35 1 2 22-8P4R-04 NPRD1
LPT D0 3 4 NPRD0
LPT AFD L 5 6 -NAFD
LPT STB L 7 8 -NSTB

LPT D7 RN37 1 2 22-8P4R-04 NPRD7
LPT D6 3 4 NPRD6
LPT D5 5 6 NPRD5
LPT D4 7 8 NPRD4

LPT D3 RN36 1 2 22-8P4R-04 NPRD3
LPT SLIN L 3 4 -NSLIN
LPT D2 5 6 NPRD2
LPT INIT L 7 8 -NPINIT



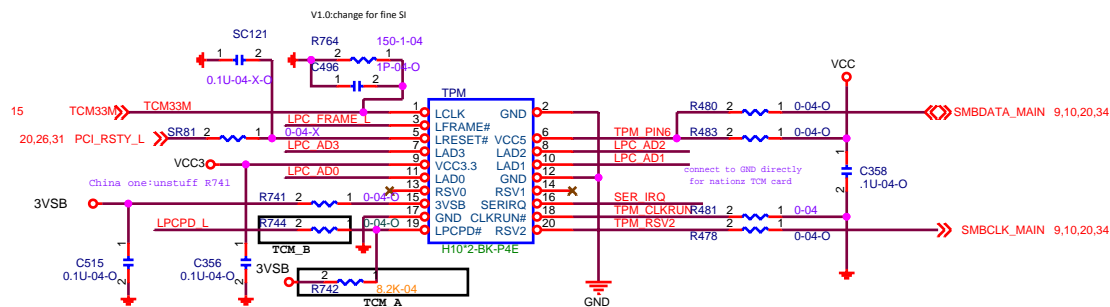
LPT Header Circuit

TPM CHIP/Header Circuit

14,26 LPC_AD[0..3] >> SB SIO
Connect SB SIO

LPCPD_L >> LPCPD_L 14
SER_IRQ >> SER_IRQ 13,26
LPC_FRAME_L >> LPC_FRAME_L 14,26

11'1017 Anny
remove colay TPM Chip circuit



V1.0:change for Nations TCM Card

BOM Difference

	TP/FDR TCM	Normal TCM
TCM_A	v	x
TCM_B	x	v

* V:stuff
X:NC

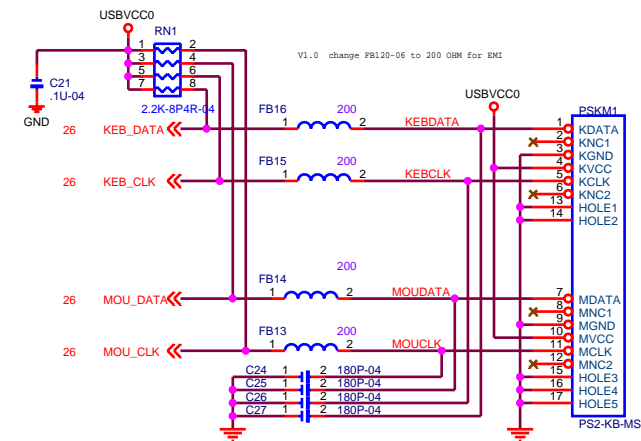
nations TCM Card note: keep pin 13,14,6,15,20 no connect

BOM Difference

	china one	other customer
R481	0 08M	check TCM Card spec

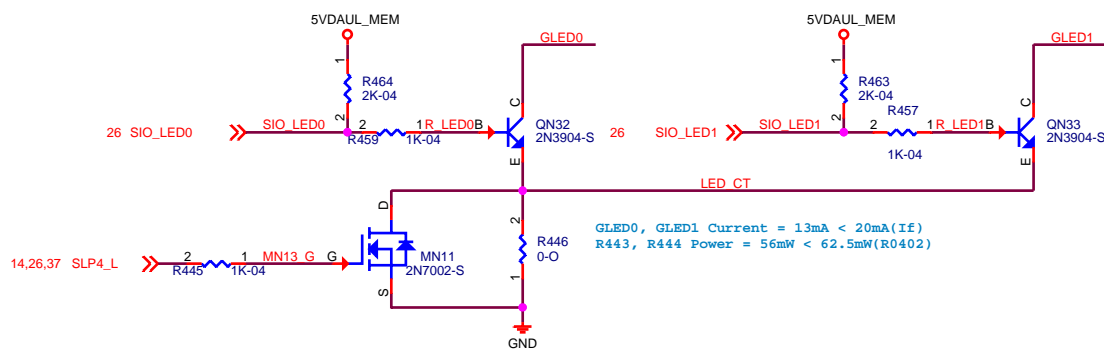
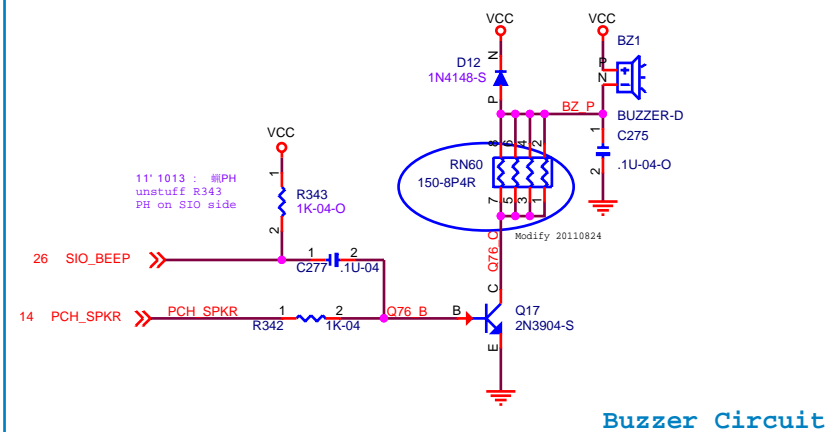
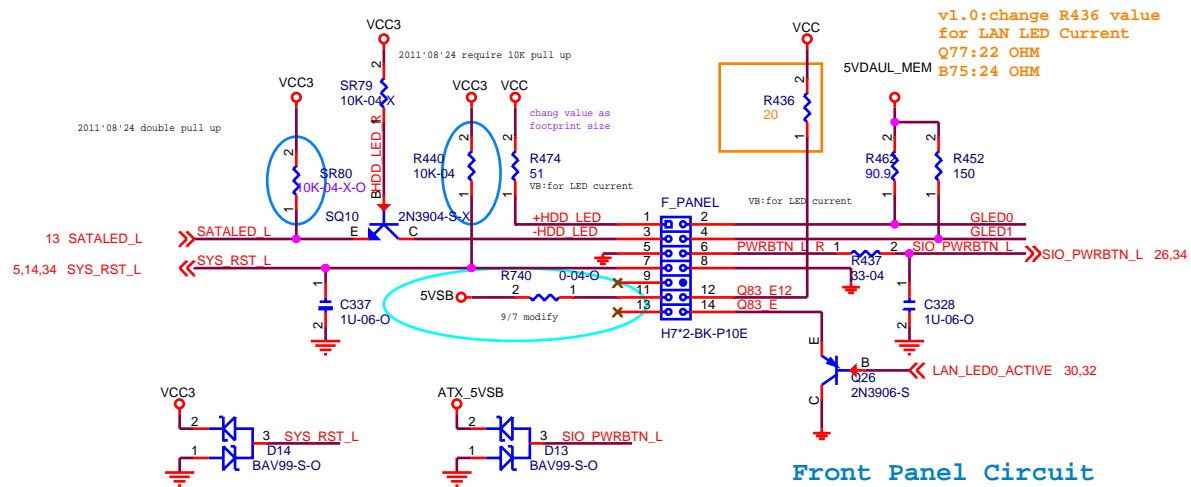
*

PS2-KB Circuit



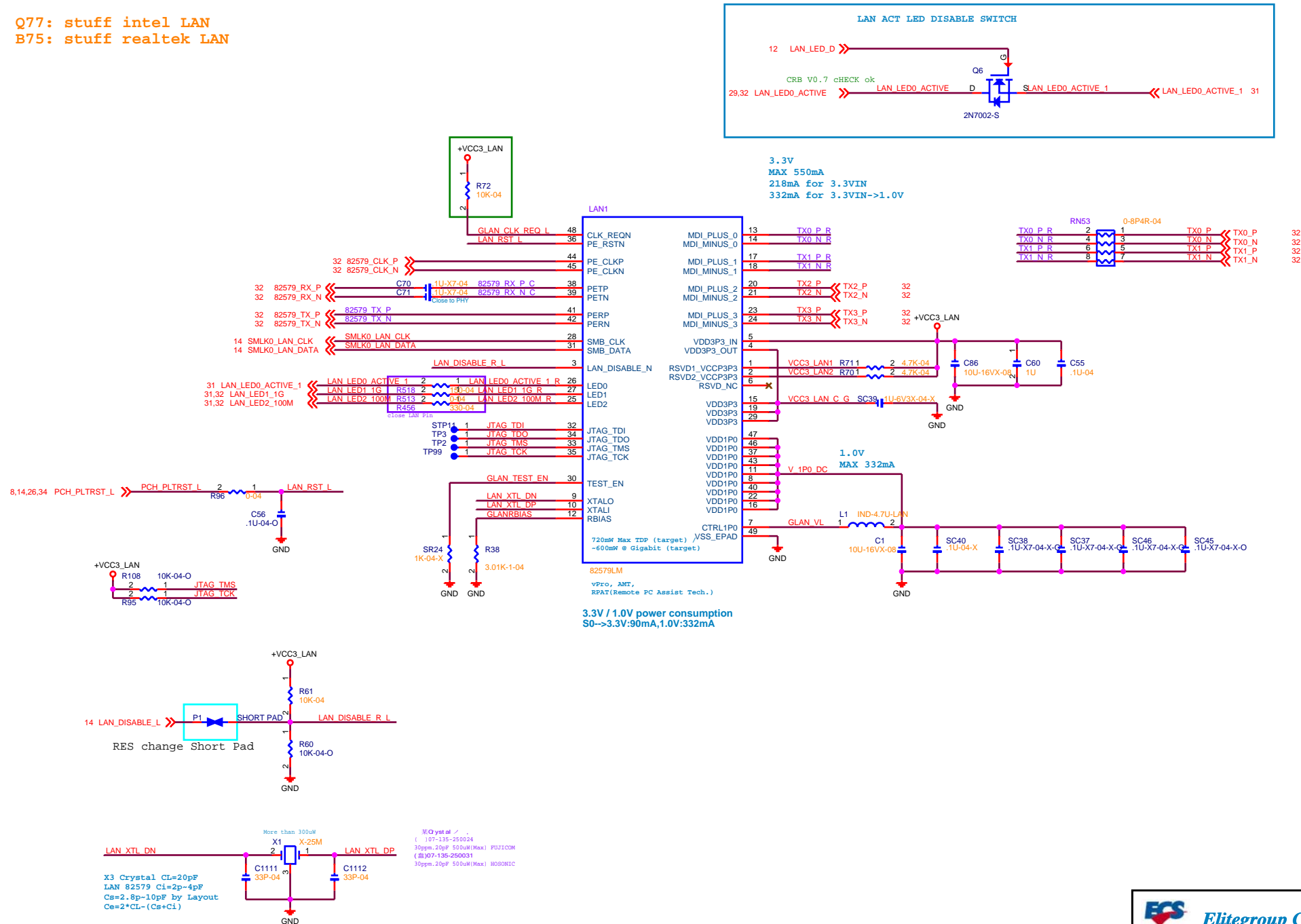
Elitegroup Computer Systems

TPM, PS/2, LPT		
Size	Document Number	Rev
Custom	Q77H2-AM2/B75H2-AM2	1.0.
Date:	Thursday, April 19, 2012	Sheet 28 of 45

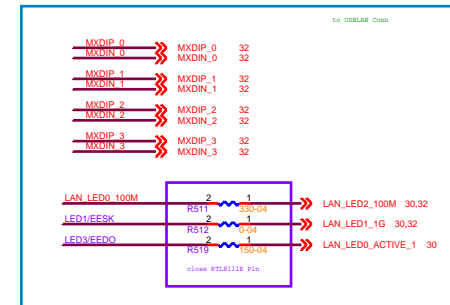
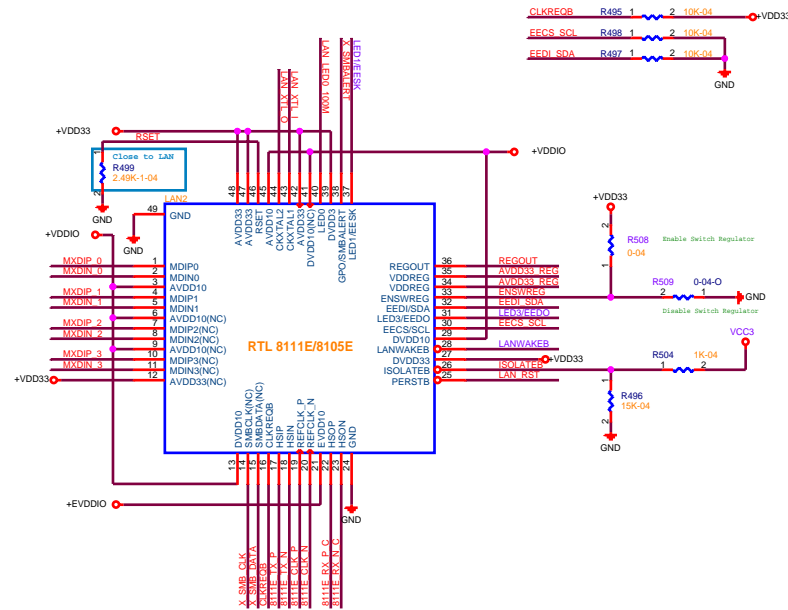
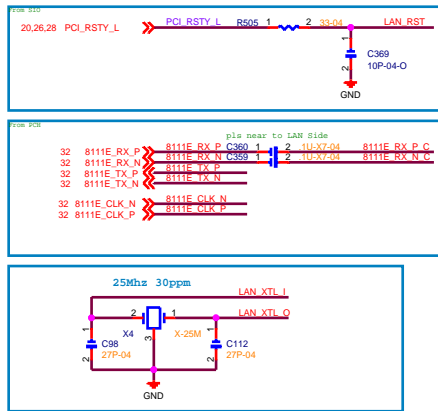


	LED	S0	S1	S3	S4/S5
Front Side	PWR LED (Single Color)	Always ON	Always ON	Blinking	OFF
	Storage LED (Single Color)	Access: Blink Others: OFF	Access: Blink Others: OFF	OFF	OFF
	LAN LED (ACTIVE) (Single Color)	Access: Blink Others: OFF	Access: Blink Others: OFF	OFF	OFF

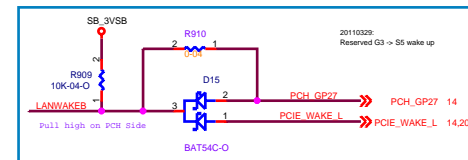
```
Q77: stuff intel LAN
B75: stuff realtek LAN
```



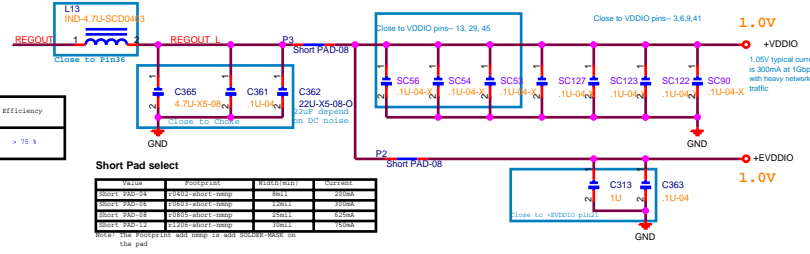
```
Q77: stuff intel LAN
B75: stuff realtek LAN
```



V1.0 :B75 unstuff D15,stuff R910;
Acer need have a dedicate GPIO
pin of SB than Wake# pin for
Onboard LAN wake up



POWER IND.4.7uH.10% 1.9A.80m OHM...SMD.4.5*4*3.2mm.FP10403F-4R7K...LEAD-FREE(ROHS/HP).TAI-TECH



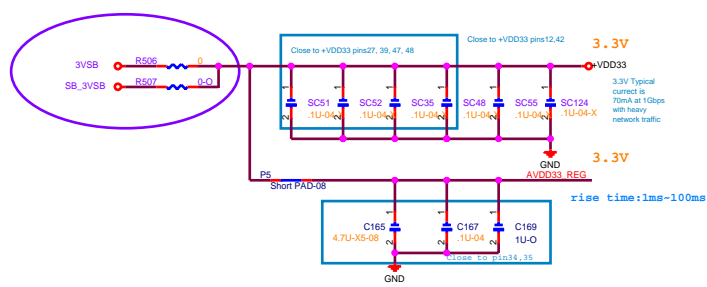
The power inductor SPEC.

L(μH)/ tolerance	ESR(ΩHz) @ 100Hz	Max. IDC (mA)	Efficiency
2.2 or 4.7 / <=20%	< 0.8	> 600	> 75 %

Short Pad select

Value	Footprint	Width(mm)	Current
Short PAD-04	R0402-short-nmnp	8mil	200mA
Short PAD-06	R0603-short-nmnp	12mil	300mA
Short PAD-08	R0805-short-nmnp	25mil	625mA
Short PAD-12	R1206-short-nmnp	30mil	750mA

Note: The Footprint add nmap is add DOLLAR-PACK on the pad

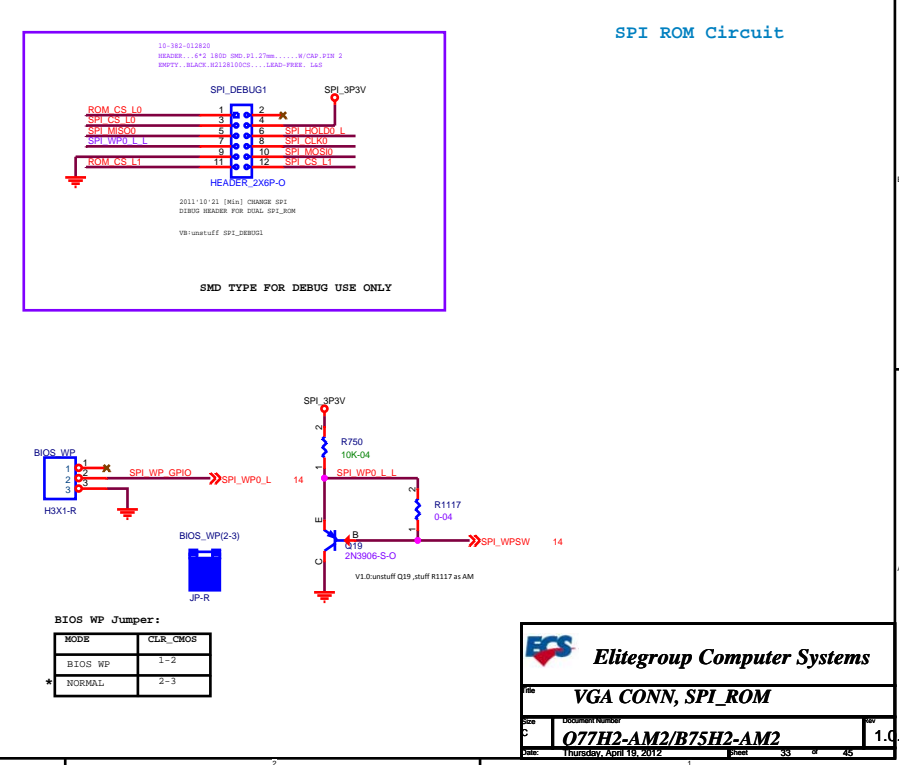
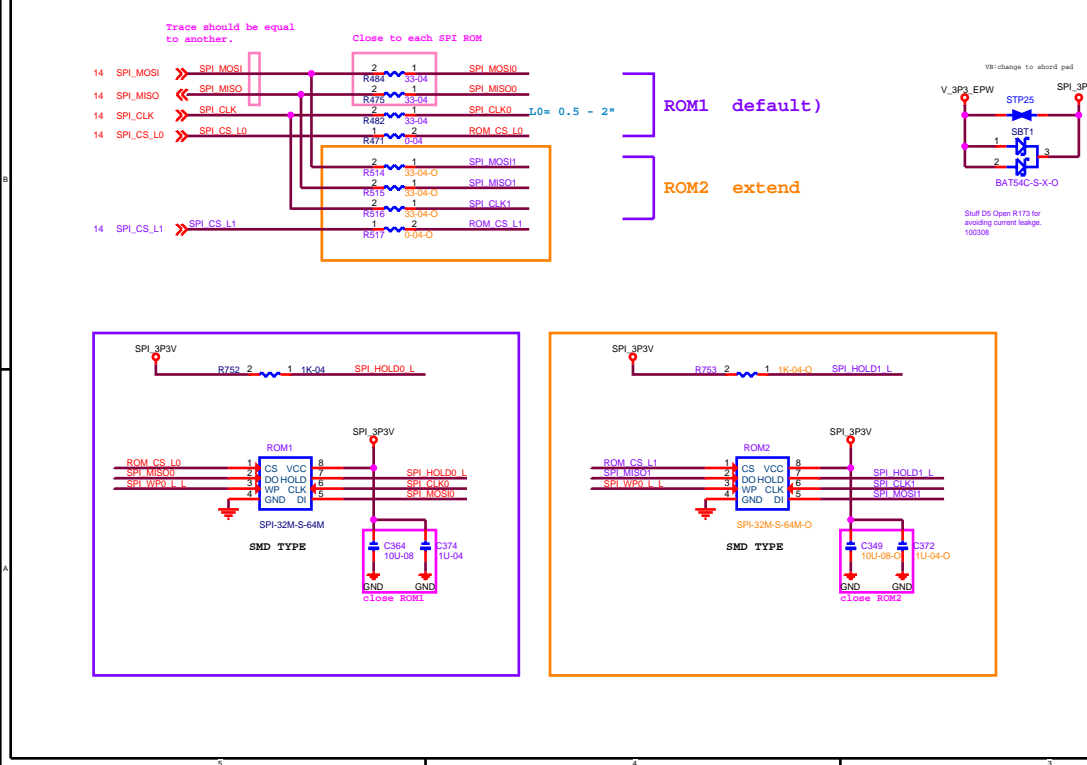
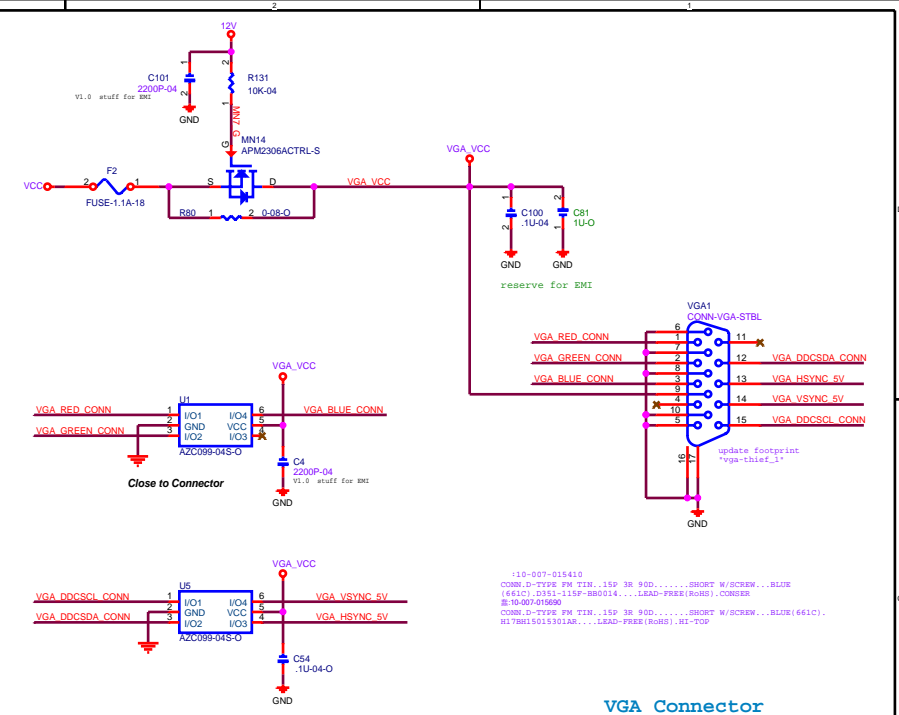


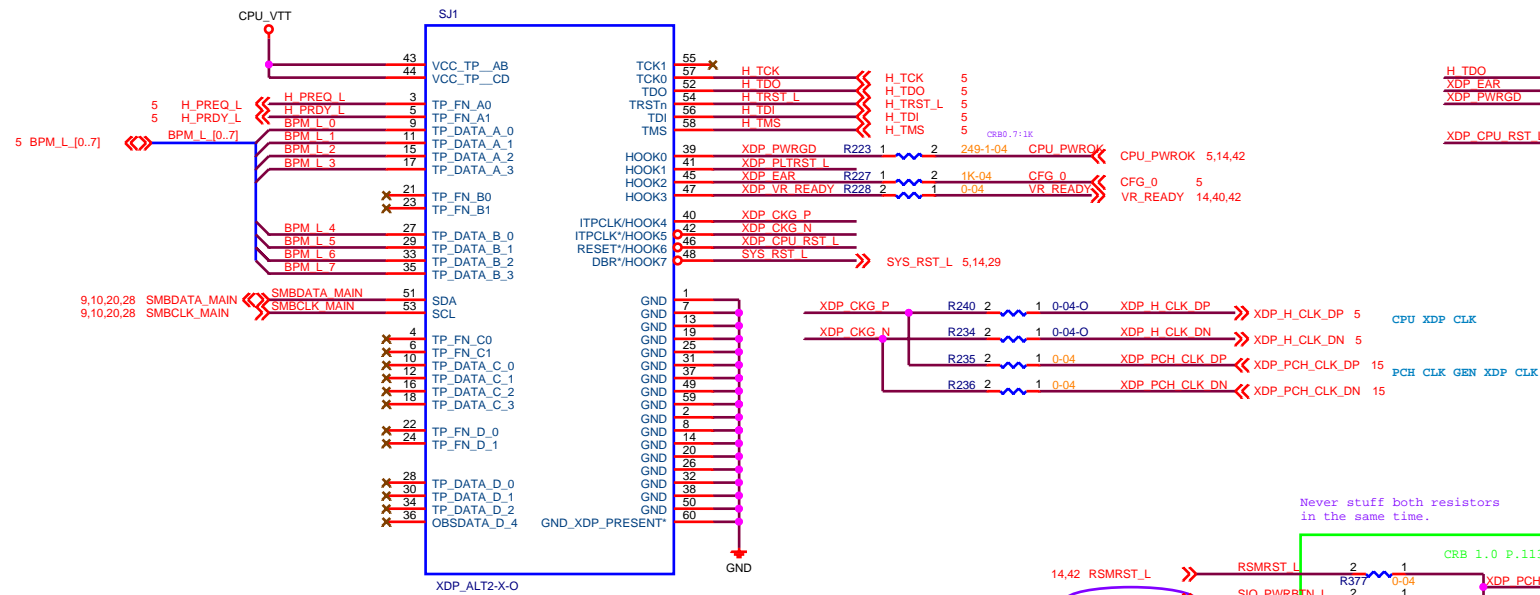
```
BOM Different between RTL8111E,RTL8105E:
For RTL8111E Series
*VDD10 pins-- 3, 6, 9, 13, 29, 41, 45.
For RTL8105E-VB
* VDD10 pins-- 3, 13, 29, 45.
For RTL8105E Series (except for VB)
* VDD10 pins-- 13, 29, 45.
```

```
BOM Different between RTL8111E,RTL8105E:
For RTL8111E Series
*VDD33 pins-- 12, 27, 39, 42, 47, 48.
For RTL8105E-VB
*VDD33 pins-- 27, 39, 42, 47, 48.
For RTL8105E Series (except for VB)
*VDD33 pins-- 27, 39, 47, 48.
```

```
Acer/FDR request:
1:default use e-FUSE;
2:only reserve External EEPROM;
3:K78 LWF/HLS111E-VL-C2 n/support ASF 2.0;
```

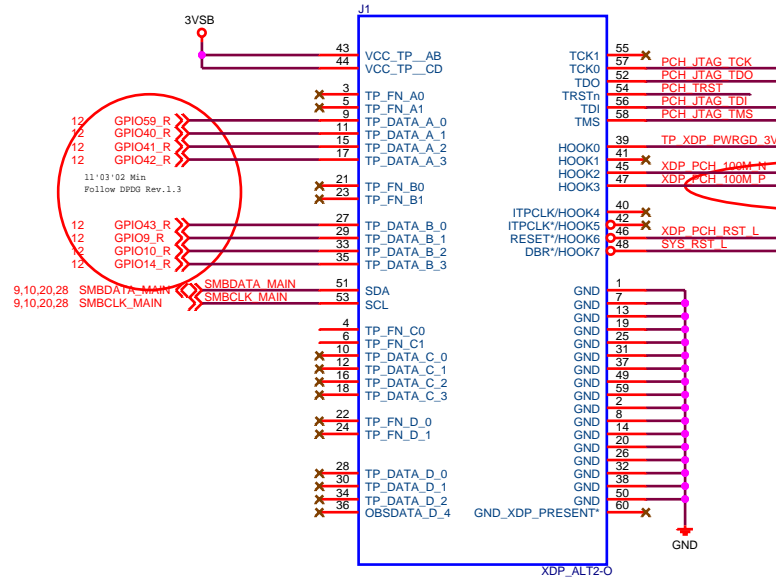






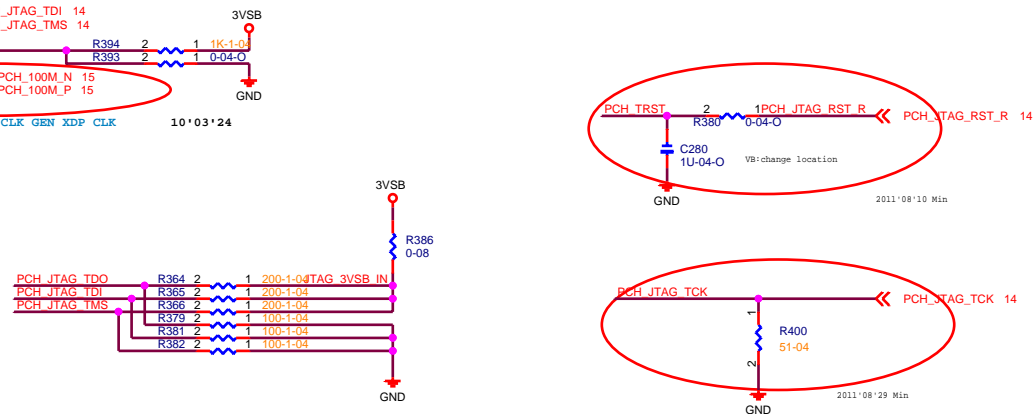
XDP Footprint:
2x30_xdp_conn for Stuff XDP
2x30_xdp_conn-nmnp for Reserve XDP

v1.0:update J1&SJ1 footprint to "2x30_xdp_conn-nmnp"

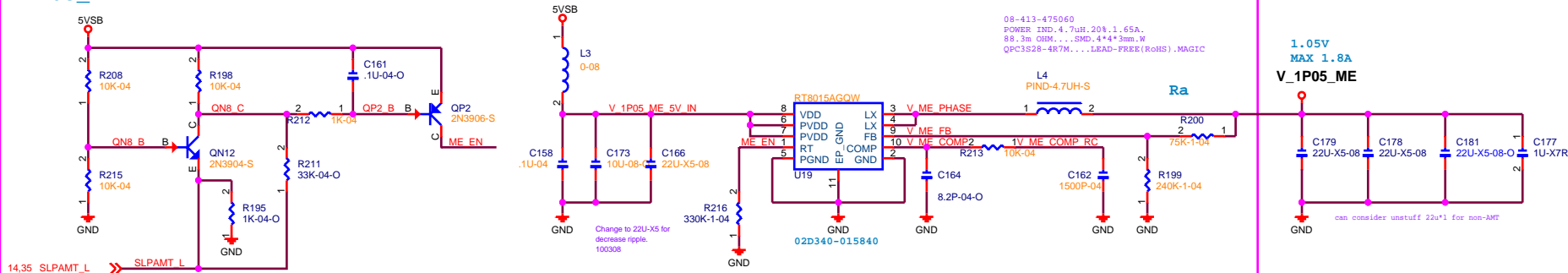


DESIGN NOTE:
PCH JTAG

DESIGN NOTE:
DEFENSIVE DESIGN



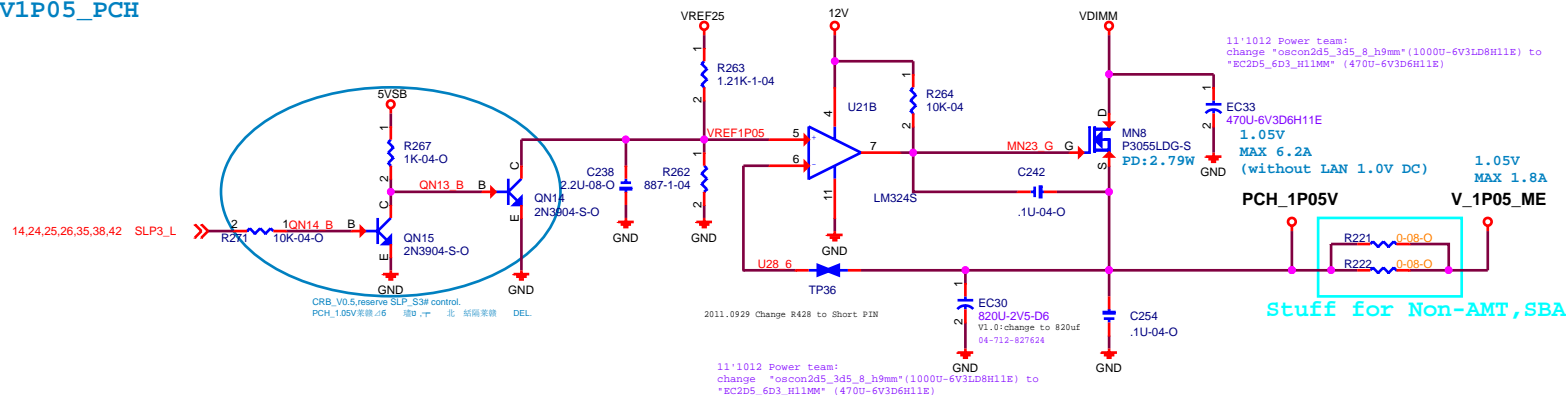
V1P05_ME



Stuff for AMT, SBA
Q77: support AMT
B75: support SBA

Ra	V_1P05_ME
75K	1.05V
90K	1.1V

V1P05_PCH



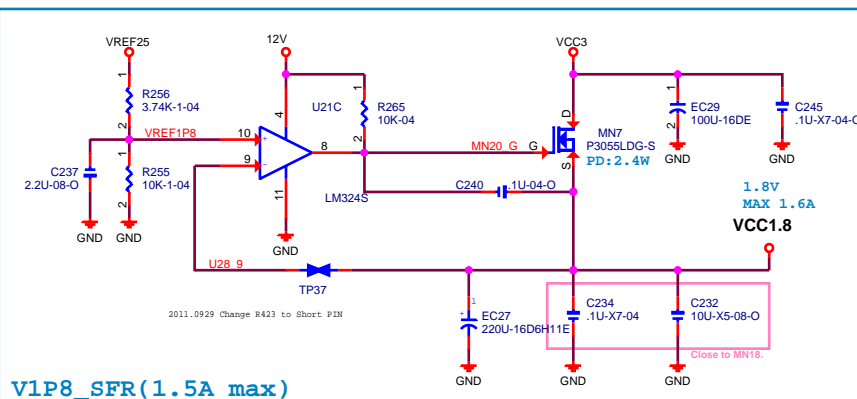
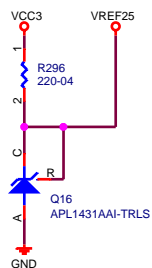
BOM Note:

02-340-015840...dn10, r8106a
IC REG RT8015AGOW.WDFN 10P.3A, LEAD-FREE(RoHS/HF).
RICHTER

04-880-828100
C/C 8.2pF, 50V, 0.25pF, NPO...SMD 0402...LEAD-FREE(RoHS/HF).

06-152-240114
RES.240K, 1/16W, 1%, SMD 0402...LEAD-FREE(RoHS/HF).

VREF25



V1P8_SFR (1.5A max)

VDIMM

BOM Different

	Ra	Rb
RT8116A	9.1K	10nF
RT8120F	16K	3.3nF

SLP4_L	High	Low
RT8120F	Enable	Disable

RT8120F & RT8116 pin to pin.
RT8116: boot voltage 30V.
02-436-116790
IC PWM RT8116AGS_SOP 8P 0.8V...LEAD-FREE
(RoHSHP) RICHTEK
RT8120FGS
IC PWM RT8120FGS_SOP 8P 0.8
V...HF LEAD-FREE RICHTEK

when the comp voltage is <0.4V, the RT8116 will be disable.
Double pole = 5.3KHz @1uH/8200P
Double pole = 4.0KHz @1uH/8200P*2
Double pole = 3.2KHz @1uH/8200P*3
Z1 = 2.27K @1.8K/.039U SS=2.0ms
P1 = 157K @1.8K/560P

2011.0913 Modify footprint
for New Regulation

Layout Note:

EC43, EC48.
Dual Value / Footprint:
560U-6V3D-OS-J / EC3D5, 6D3_H9MM
560U-6V3D-OS-J / EC3D5, 8_H9MM_1P

1.5V
MAX 22A
OCP:36.7A

Layout Note:

VSMCx are under Channel B.
VSMCy are between Channel A & B.
VSMCz are between Channel A & CPU.

DDR_VTT

CSB RESERVE S3 CTRL CKT

02-344-337700 APL5337KAI-TRG instead of APL5336
02-345-172891 AME9172M-AZA
02-345-101910 NCT3101S

10'07'09
change footprint

0.75V
MAX 1A
Pd:0.75W



Layout Note:
SMVTTcf close to U35 Pin4.
SMVTTcg are between Channel A & B.
SMVTTch are between Channel A & CPU.

close to IC

CHECK FOOTPRINT

Elitegroup Computer Systems

DC/DC VDIMM/DDR_VTT

Size Document Number

Custom

Date: Thursday, April 19, 2012

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Q77H2-AM2/B75H2-AM

VCCSA

Stuff VSAGz

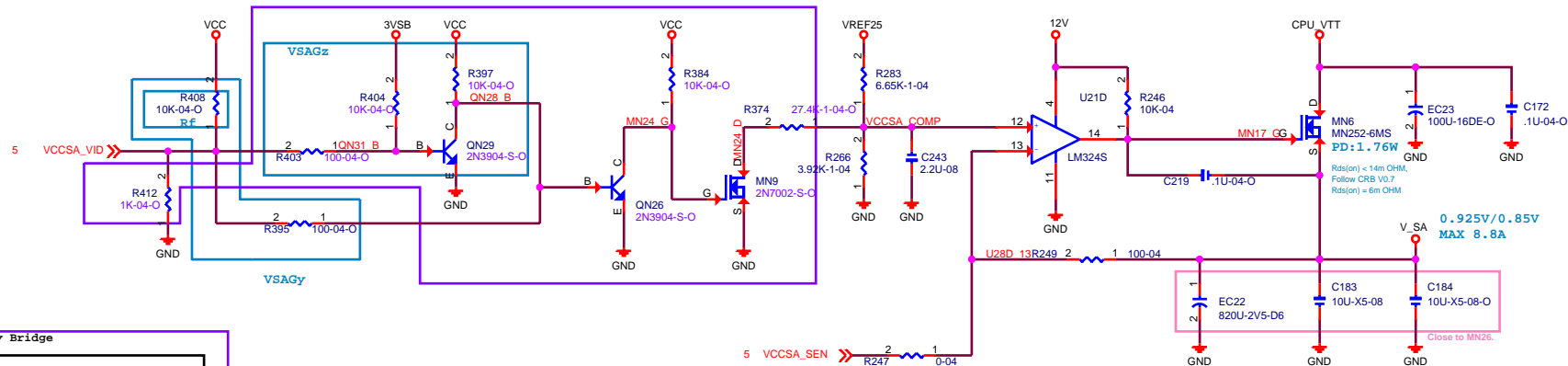
VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V

Stuff VSAGy

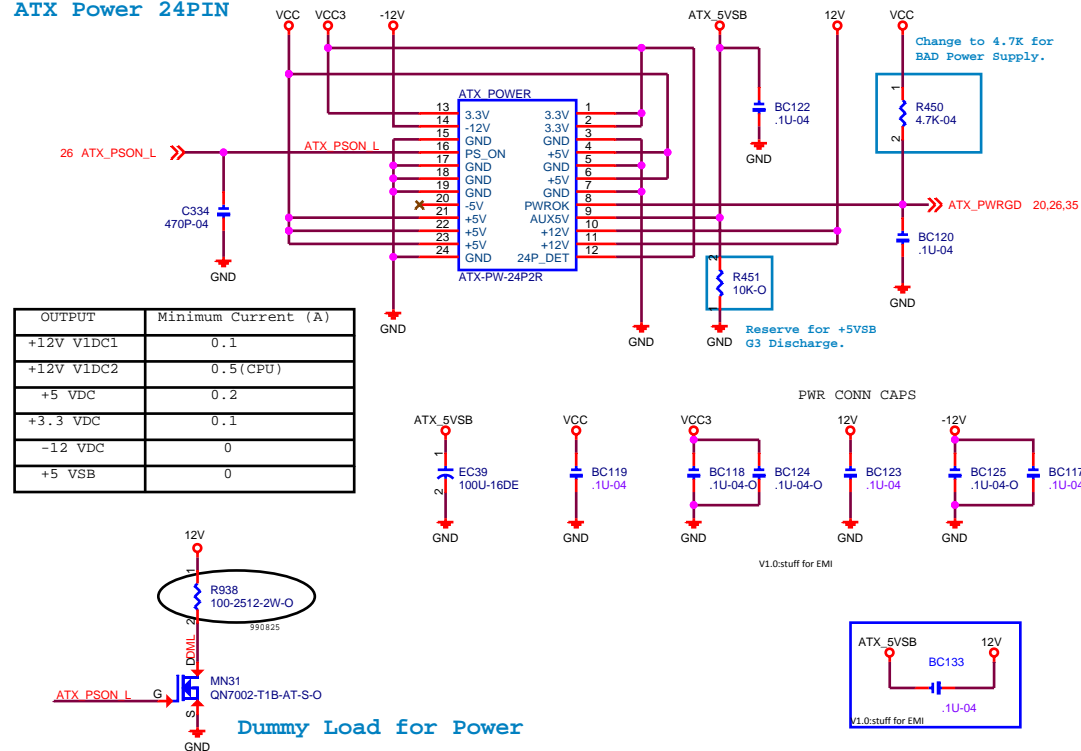
VCCSA voltage selection	
Rf	+V_SA
unstuff	0.85V
stuff	0.925V

WW23 Intel POR VCCSA=0.925V for IVY/Sandy Bridge

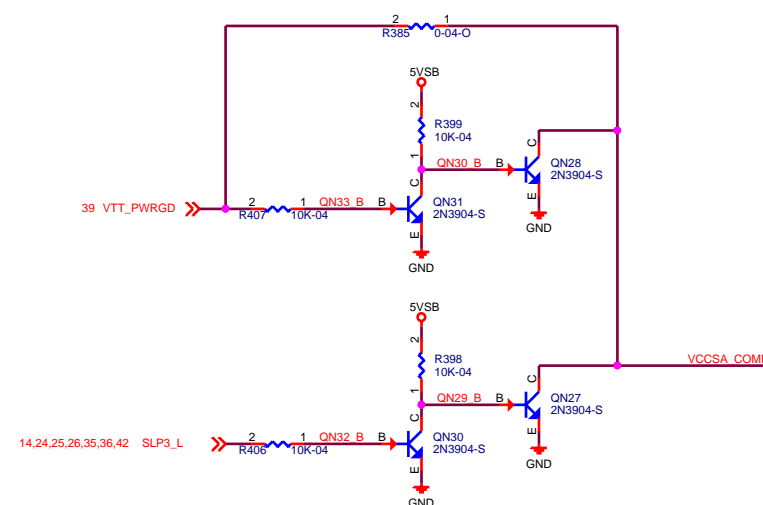
VCCSA Voltage Selection		
	0.925V	0.85V
CPU(ES1 sample)	stuff A(control by VCCSA_VID)	
CPU(ES2 sample)	Sandy=>VCCSA_VID=0;	X
CPU(QS)	Ivy=>VCCSA_VID=0;	
	Unstuff A(default)	X



ATX Power 24PIN

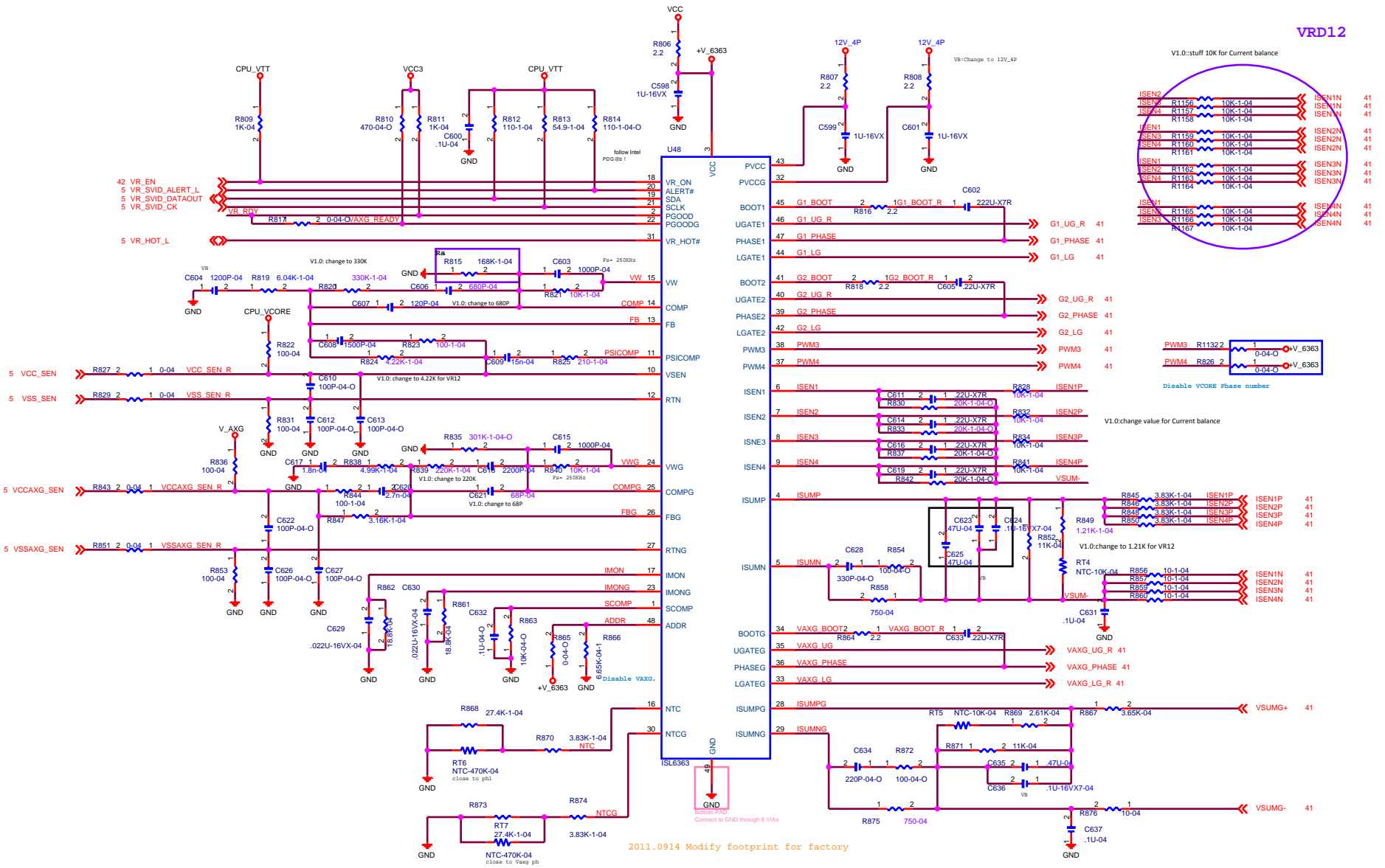


VCCSA Sequence



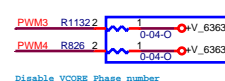
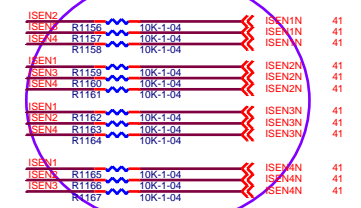
Elitegroup Computer Systems

DC/DC VCCSA, ATXPWR	
Size	Document Number
Custom	Q77H2-AM2/B75H2-AM2
Date	Thursday, April 19, 2012
Sheet	38 of 45

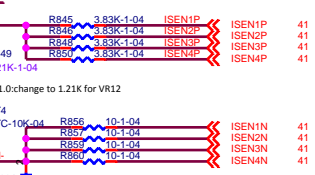


VRD12

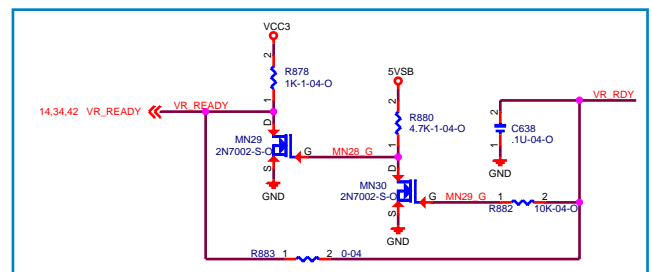
V1.0:stuff 10K for Current balance



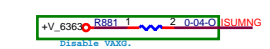
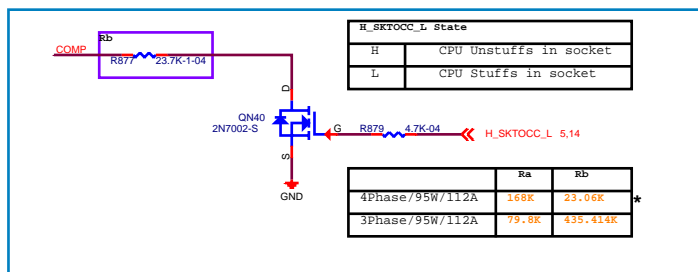
V1.0:change value for Current balance

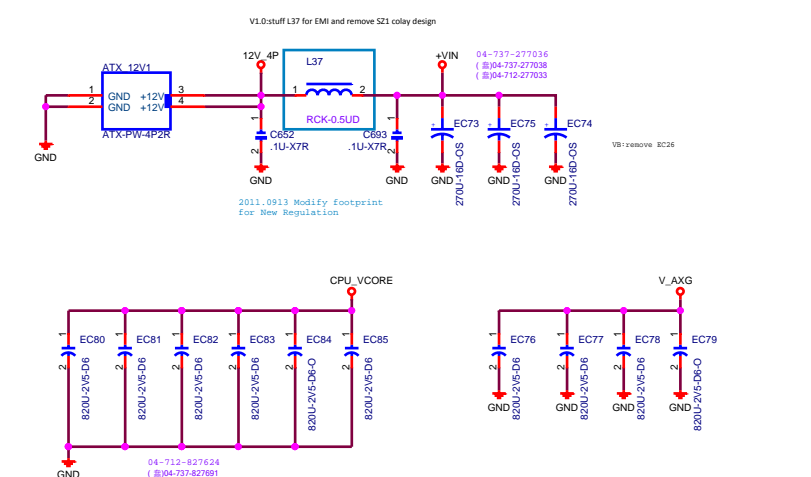
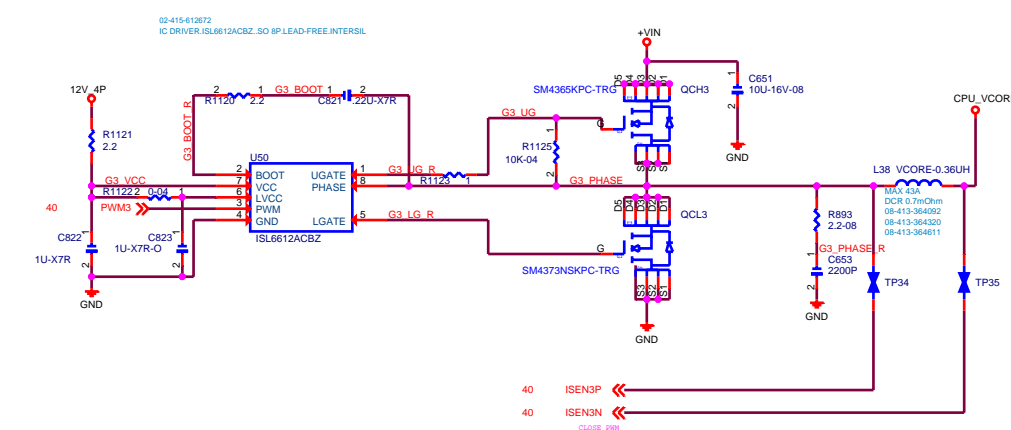
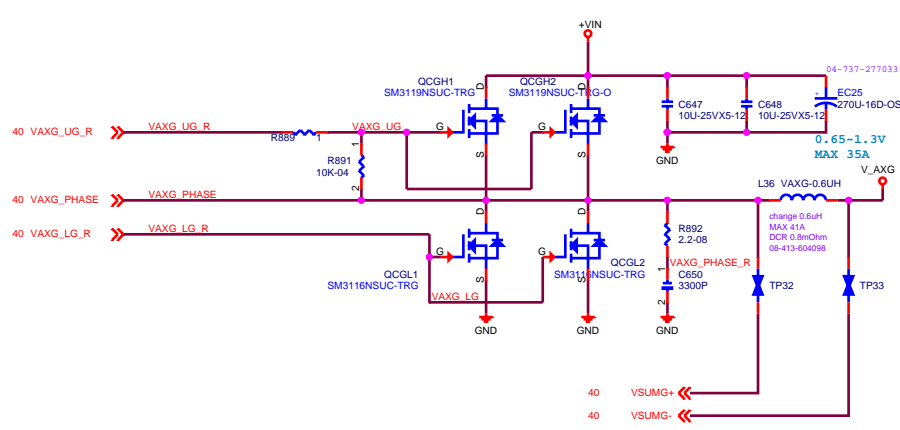
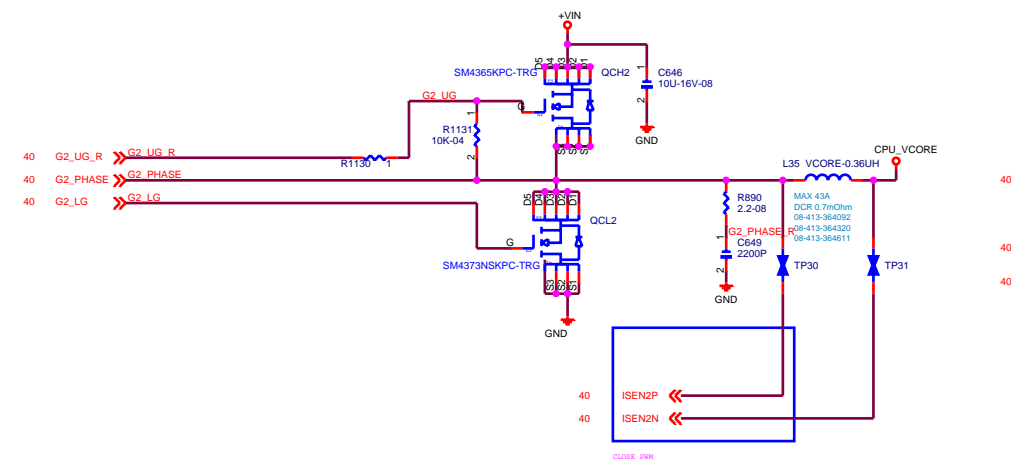
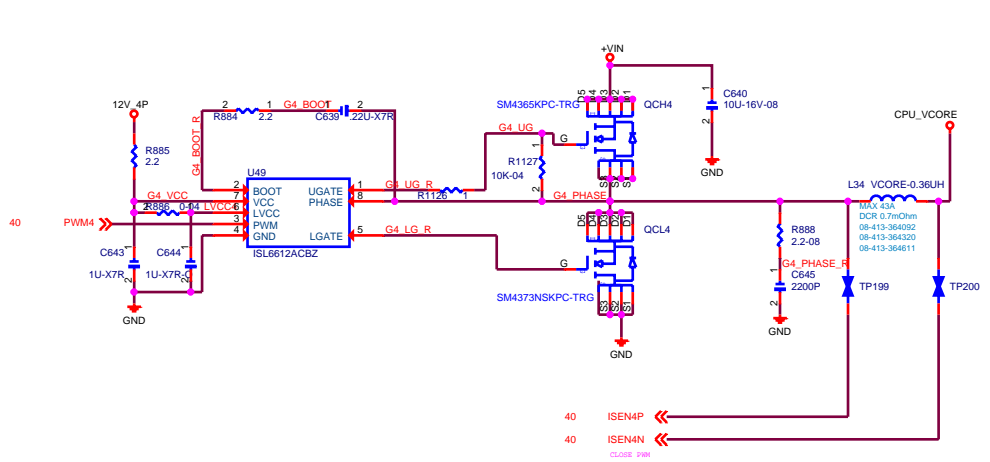
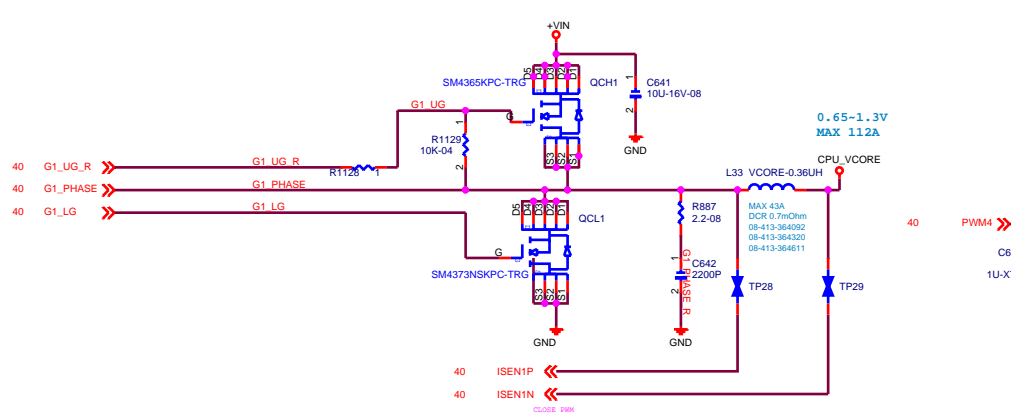


2011.0914 Modify footprint for factory



For VR_READY Power On Sequence





ATX P/S WITH 1A STBY CURRENT					
5VSB	5V	3.3V	12V	-12V	
+/-5%	+/-5%	+/-5%	+/-5%	+/-5%	

ATX4P
12V
+/-5%

Switching
ISL6363
4+1 phases

Switching
ISL5870B
1 phase

Switching
NCP1587

DDR3 DIMM (4) 1333MHz	
VDDQ	15A_S0
V_SM_VTT	1.0A_S3

Linear
LM324

LDO
APL5336

Linear
LM324

Intel Ivy Bridge CPU			
VCCP	VIB 0.25~1.52V	TDC :85A(95W)	
VAXG	VIB 0.25~1.52V	25A	
VTT	1.05V(1V)	8.5A	
VCC_SA	0.925V(0.85V)	8.8A	
VCCPLL	1.8V	1A	
VDDQ	1.5V	4.75A	

Intel Panther Point (TDP 5.5W)			
V_PROC_IO	1.05V	2mA	
VccDMI	1.05V	0.057A	
VccCORE	1.05V	2.52A	
VccIO	1.05V	4.57A	
VccADPLLA	1.05V	0.1A	
VccADPLLB	1.05V	0.1A	
VccCLKDMI	1.05V	0.08A	
VccSSC	1.05V	0.105A	
VccDIFFCLKN	1.05V	0.055A	
VccASW(ME)	1.05V	1.61A	
VccDFTERM	1.8V	0.2A	
VccVRM	1.8V	0.185A	
Vcc3_3	3.3V	0.409A	
VccADAC	3.3V	0.068A	
VccSPI	3.3V	0.02A	
VccDSW3_3	3.3V	0.003A	
VccSUS3_3	3.3V	0.1A	
VccSUSHDA	3.3V	0.012A	
VccRTC	3.3V	6uA(G3)	
V5REF	5V	1mA	
V5REF_SUS	5V	1mA	

Fans
12V_200mA

SPI
VCC3_30mA

CRT
VCC_1A fuse

HDMI/DP
VCC3_0.5A fuse x 2

HDMI L.S.
VCC3_180mA

Flash/NVM
VCC3_0.3A
1.8V_0.1A

Battery
3V

B75

LAN INTEL_82579			
VDD3P3	3.3V	90mA	
VDD1P0	1V	332mA	
CTRL1P0 internal LVR Output			

REALTEK RTL8111E_VL			
VDD3P3	3.3V	70mA	
VDD1P0	1.0V	300mA	
CTRL1P0 internal LVR Output			

SUPER I/O IT8728 FX			
3VSB	3.3V	< 6mA (S0/S1/S3/S4/S5)	
VCC3	3.3V	< 10mA (S0/S1)	
BAT 3.3V	3.3V	<< 2 uA (S0/S1/S3/S4/S5)	

AUDIO ALC662-VD			
DVDD 3.3V	3.3V	23mA	
AVDD	5V	38mA	

LDO


Elitegroup Computer Systems

Power Delivery	
Document Number	Q77H2-AM2/B75H2-AM2
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Maho Bay Platform has two clock mode:
 1. Integrated Clock Mode (Generate by PCH)
 2. Buffer Through Mode (Generate by Clock Gen.)
 If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.
 Please refer to
 Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD
 Page.13 PCH - SATA, SATA CONN for CLK IN PD
 Page.14 PCH - MISC, F/W Strap
 Page.15 PCH - CLK IO, CKG

